NOVEL NANOMANUFACTURING METHODS FOR BOTTOM-UP III-V NANOWIRES AND VAN DER WAALS EPITAXY OF MONOLAYER M_OS_2

BY

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DISSERTATION

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ABSTRACT

Nano materials such as nanowires and 2-dimensional (2-D) molybdenum disulfide (MoS_2) have received tremendous attention over the past few decades. Numerous applications have been proposed such as nanowire MOSFETs, nanowire electrical generators, nanowire biosensors, nanowire single photon detectors, MoS_2 transistors, and MoS_2 photodetectors. Some of these devices outperform state-of-the-art commercial products, but none of these nano material based devices have been commercialized up to date. One of the biggest barriers for industries to use these nano materials is a lack of mass fabrications methods. For nanowires, obtaining a large area planar array of nanowires is extremely difficult and no known method can achieve a high-density large-area array of precisely positioned nanowires. Although there has been huge progress over the past few years, the yield and density of planar nanowire arrays from the reported literature are far from required values for industrial use. For MoS_2, obtaining a single-crystal phase with a wafer-scale uniform monolayer is needed in order for the material to be mass fabricated. Although wafer scale monolayer MoS_2 has successfully been grown, it contained a high density of grain boundaries which would cause non-uniform performance when mass produced into nano-scale devices.

In this dissertation, general pathways for commercialization of nanowire and MoS_2 based devices will be explained as well as the backgrounds on the nanowire/MoS_2 field. Also, state-of-the-art methods for achieving planar nanowire arrays and growing monolayer MoS_2 will be discussed. In a later section, a new method will be proposed that shows the highest yield and density of planar nanowires ever reported. A growth method for obtaining large-scale single-crystal monolayer MoS_2 will be proposed as well.

To my family

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CHAPTER 1 – INTRODUCTION

1.1 Vapor-Liquid-Solid (VLS) Growth of Nanowires

There are various reported methods for fabricating nanowires such as the VLS method [1], solution-based growth [2], physical vapor deposition growth method [3], metal assisted chemical etching method [4], and chemical etching [5]. In general, these nanowire fabrication methods can be categorized into either top-down or bottom-up approaches [6]. A top-down approach etches a large material down to nanowires by lithography and chemical/physical etching whereas the bottom-up approach grows nanowires from the bottom up by using atomic sources (Figure 1.1). Although the top-down approach is simple and allows precise positioning of the nanowires, there are many advantages of bottom-up growths. First, bottom-up growth results in a much smoother surface compared to the top-down approach. Because rough surfaces act as scattering centers in electrical devices, obtaining an atomically smooth surface enhances device performance greatly. Second, unlike in top-down approach, lattice mismatched nanowires without defects can be grown. Third, geometries that are very difficult to make by the top-down approach can be made easily. Structures such as core/shell nanowires and nanowire superlattices can be easily grown by the bottom-up approach but are hard to be fabricated by the top-down approach.

Vapor-liquid-solid (VLS) growth is the most commonly used bottom-up method for growing semiconductor nanowires. In a VLS growth, the “vapor” phase source gets into the “liquid” phase particles and precipitates out to form “solid” phase crystals. Metal catalysts such as gold or nickel are most commonly used for the VLS growths. The size of the nanowires grown by the VLS method is determined by the size of these metal catalysts used.

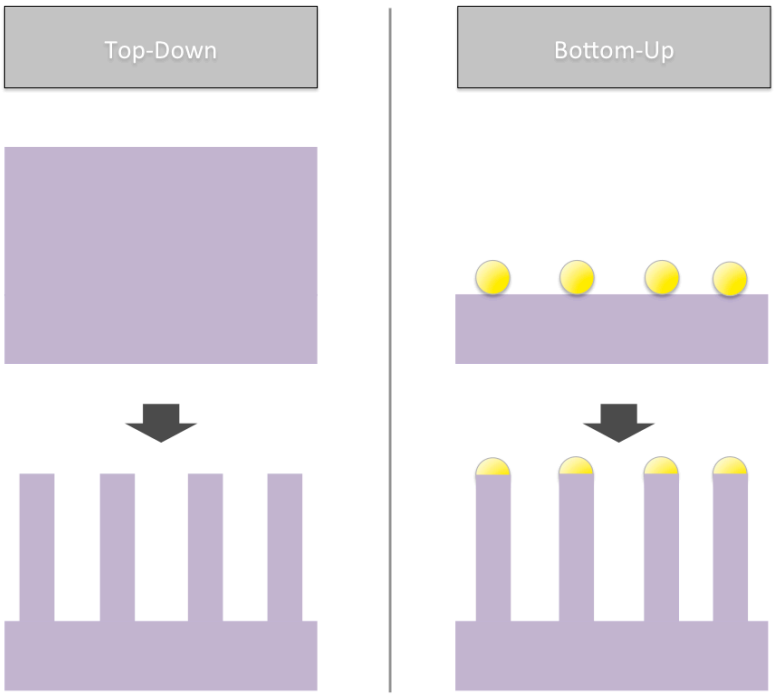

Figure 1.1 Comparison between top-down and bottom-up approaches of nanowire fabrication.

Growth direction of the nanowires are determined by the surface energy of the crystal facets, interface energy between the nanowire and the catalyst, and the local Gibbs energy during the growth of the nanowires. Although growth of nanowires in various directions has been reported, under most of the conditions, nanowires with cubic crystal structures tend to grow in <111> directions and those with hexagonal crystal structures tend to grow in <0001> directions. For III-V semiconductor materials such as InAs, GaAs, and InP, <111> directions are categorized into either <111>A and <111>B due to the difference in terminating atoms. For example, in InAs nanowires, the (111)B surface is As terminated with one dangling bonds whereas the (111)A surface is In terminated. Thus, there is a relatively large surface energy difference between (111)A and (111)B surfaces, and in general, III-V nanowires tend to grow in <111>B directions which have lower surface energy.

1.2 State-of-the-Art Methods for Planar Alignment of Nanowires

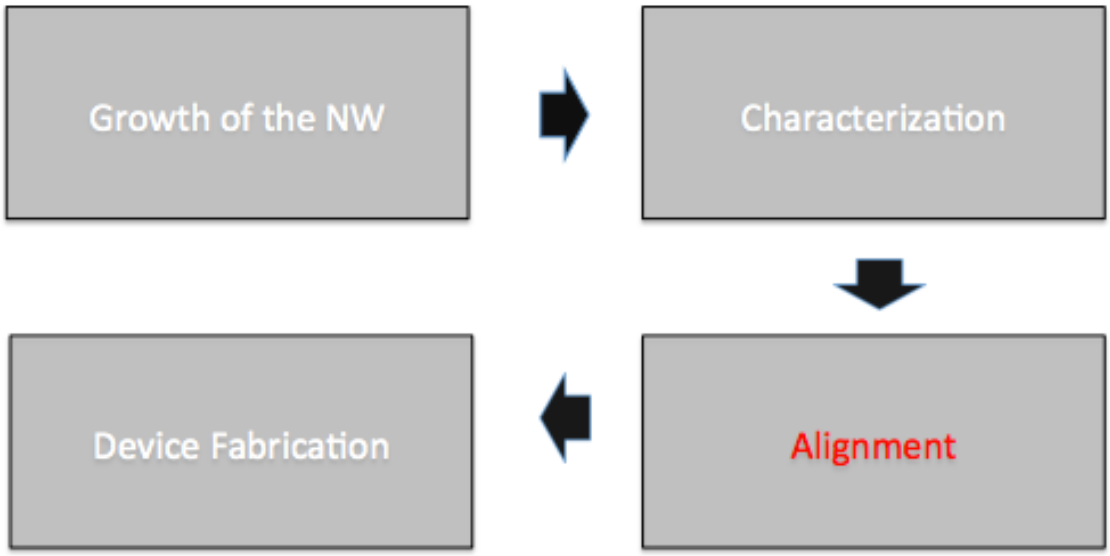

Figure 1.2 Process flow for mass production of nanowire-based devices. A nanowire alignment process suitable for mass production has not been established to date.

Since the VLS growth of nanowires (microwhiskers) was first reported by Wagner in the 1960s [1], nanowires have been extensively researched and numerous applications have been proposed. In order for the nanowire-based devices to be actually commercialized, nanowire growth needs to be first optimized in order to acquire the right dimension and crystal structure for a desired device. Characterization of the grown nanowires needs to be done thoroughly to confirm the quality of the grown nanowires. Then, the nanowires need to be aligned in large scale in planar fashion for the mass production of nanowire-based devices.

The growth and characterization of nanowires as well as fabrication of various nanowire-based devices have been extensively studied and are well established, but because many of the nanowire-based applications require a large area planar alignment of the grown nanowires, none of the proposed devices have actually been used in industries (Figure 1.2).

Absence of a method for achieving large-area planar arrays of VLS grown nanowires acts as one of the biggest obstacle for the commercial use of nanowire-based devices. There has been progress in nanowire aligning methods during the past few years and the yield of single nanowire arrays have reached up to 98.5% [7]. However, these methods are suitable for low-density applications only, and for high-density applications such as transistors, both the high yield and density are required. Over the past few decades, researchers have tried to achieve high density and yield of single nanowire arrays through various methods such as the selective lateral epitaxy method [8], Langmuir-Blodgett method [9], contact printing method [10], dielectrophoresis assembly [7], and nanoscale combing technique [11]. To date, dielectrophoresis assembly method has achieved highest yield of single nanowire arrays with a yield of 98.5% [7]. The dielectrophoresis assembly method, however, is limited to low-density applications with over 10 μm pitch between the nanowires. There have been reports on achieving higher densities of single nanowire arrays with pitches of a couple microns, but the yield of single nanowires per sites were significantly lower compared to dielectrophoresis assembly [11].

Various nanowire aligning methods exist in the literature, but most of the reported methods have single nanowire alignment yields that are far below the required value for industrial use. The dielectrophoresis nanowire alignment method (Figure 1.3 (a)) [7], which was reported several years ago, has achieved highest yield of single nanowire arrays with up to 98.5%, but there are several drawbacks to this method. First, because the dielectrophoresis method utilizes electric fields and electric fields from adjacent electrodes influence each other, the density of the single nanowire arrays are limited to ~1 nanowire/12 μm and thus can be used for low-density applications only such as light-emitting diodes. Second, the method requires relatively complex

fabrication of microfluidic channels and electrodes. Third, position error of the aligned single nanowires are relatively high with ±100 nm from the center of each electrodes.

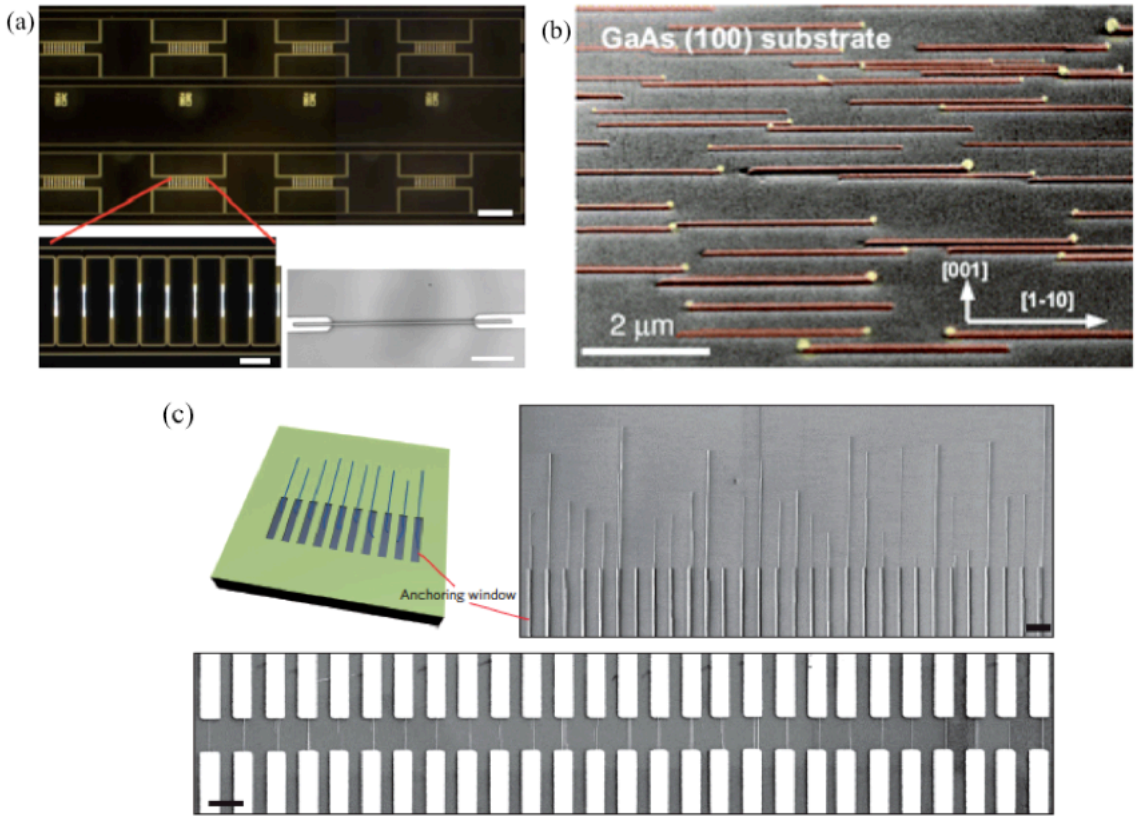

Figure 1.3 Various nanowire aligning methods. (a) Dielectrophoresis method, (b) selective lateral epitaxy alignment, (c) nanocombing method. Adapted by permission from Macmillan Publishers Ltd: *Nature Nanotechnology*, Reference [7], copyright (2010). *Nature Nanotechnology*, Reference [8], copyright (2013). Adapted with permission from Reference [11]. Copyright (2008) American Chemical Society.

Selective lateral epitaxy of nanowires (Figure 1.3 (b)), in comparison with dielectrophoreis method, is more simple, precise, and higher in density [8]. The only fabrication step required for the alignment is the patterning of Au catalysts for the nanowire growth, and the positions of the nanowires are precisely controlled by the position of the Au dots patterned through lithography steps. Also, since the alignment of the nanowires are guided by the substrate epitaxially, the crossing defects of nanowires cannot occur and the misalignment angle of the aligned nanowires

is 0˚. There is no limit for the density of the nanowires for this method. However, because of the epitaxial nature of the aligning method, material selections are limited and mismatched planar nanowire growth results in significantly lower yields of the single nanowire alignment. Also, homoepitaxial growth of planar nanowires such as InAs cannot be fabricated into devices even with selective doping into the nanowires since the bandgap of the material is too small and thus semi-insulating wafers do not exist.

The advantage of the nanoscale combing technique (Figure 1.3 (c)) is that it can achieve a relatively high density of nanowires (~2 μm distance between the aligned nanowires) [11], has simple fabrication steps compared to the dielectrophoresis method, and is not limited by materials, and any nanowires can be aligned into arrays. However, the highest yield of single nanowire arrays achieved by this method is only ~70%.

Thus, no known method can achieve high yield (>95%) and high density suitable enough to be applied to the semiconductor transistor industries. In the following sections, this dissertation will focus on the growth, characterization, and large-scale alignment of the nanowires as well as the device fabrication based on the array of nanowires.

1.3 Advantages of InAs Nanowires for Transistor Channel

The III-V compound semiconductors, in general, have much higher electron mobility compared to silicon. The biggest drawback of these materials which makes industries reluctant to use III-V compounds, is the cost. Bottom-up grown III-V nanowires are thus good candidates to replace silicon-based transistors in the near future.

InAs nanowires, with bulk electron mobility of ~40000 $cm^2V^{-1}s^{-1}$, are a good candidate for transistor applications [12]. Although the electron scattering increases with the decrease in

the diameter of the nanowires, studies on the effect of the diameter on the InAs electron mobility show that the InAs nanowires have electron mobility of over 16000 $cm^2V^{-1}s^{-1}$ even with 15 nm diameters [13]. Having a high electron mobility channel is especially advantageous in short channel devices since high electron mobility leads to high electron injection velocity [14]. It can be seen in Figure 1.4 that III-V materials have much higher electron injection velocity compared to silicon.

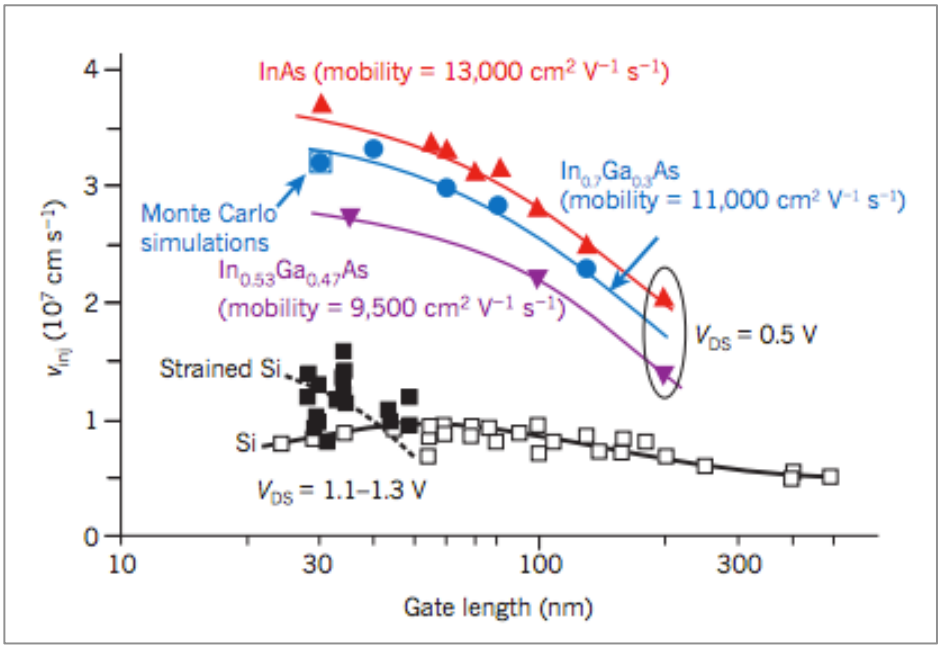

Figure 1.4 Electron injection velocity measured in III-V HEMTs. Adapted by permission from Macmillan Publishers Ltd: *Nature*, Reference [14], copyright (2011).

InAs nanowires are also advantageous for use in ballistic transistor applications. In ballistic transistors, the carriers do not scatter within the channel and thus can operate with maximum on-state conductance [15]. Because electrons have a long mean free path in InAs, room temperature ballistic operation of InAs nanowire transistors with ~60 nm channel length has been reported [16].

1.4 2-D MoS_2 Growth Methods

During the last ten years or so, 2-D materials have attracted the attention of numerous researchers due to their superb properties [17], potential in transparent electronics [18], and easier device fabrication compared to 1-D nanostructures. Among the 2-D materials, graphene has been most widely studied due to its outstanding properties [17]. However, graphene does not have a bandgap, which limits its use in many device applications. Single-layer MoS_2, on the other hand, is a direct bandgap semiconductor with a bandgap of ~1.9 eV [19]. CVD growth has been the most popular growth method for obtaining 2-D MoS_2 whereas sulfur and molybdenum oxide powders are used as precursors (Figure 1.5 (Top)). Recently, the MOCVD growth method of MoS_2 has also been reported in which $Mo(CO)_6$ and $(C_2H_5)_2S$ are used as precursors (Figure 1.5 (Bottom)).

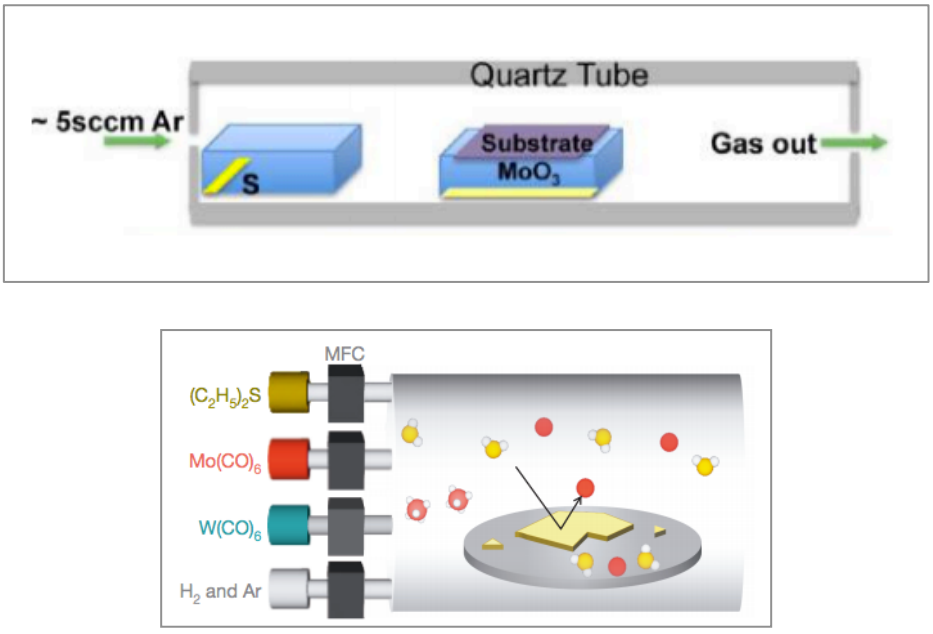

Figure 1.5 Typical MoS_2 growth methods. (Top) Illustration of the CVD method using S and MoO_3 powders. (Bottom) Illustration of the MOCVD method for growing single-layer MoS_2. Adapted with permission from Reference [20]. Copyright (2014) American Chemical Society. Adapted by permission from Macmillan Publishers Ltd: *Nature*, Reference [21], copyright (2015).

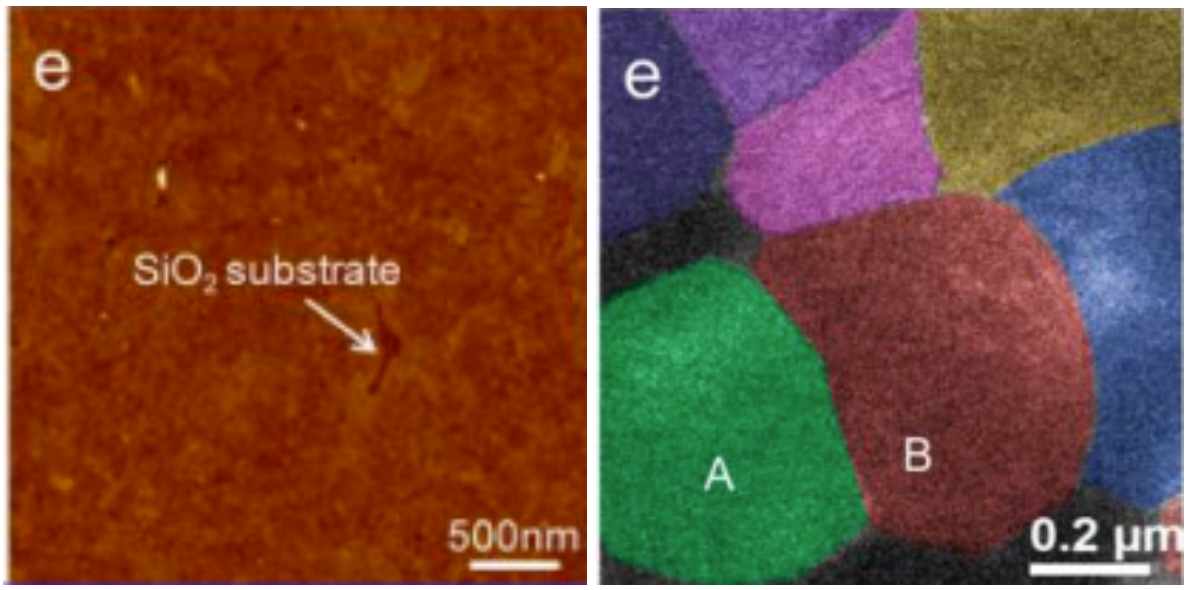

Figure 1.6 (Left) AFM image of a monolayer MoS_2 grown on SiO_2 substrate. (Right) False-color DF-TEM image of the monolayer MoS_2. Different grains are shown in different colors. Adapted with permission from Reference [22]. Copyright (2014) American Chemical Society.

Various CVD growth conditions have been reported that results in monolayer MoS_2 [23, 24]. The growth method can be categorized depending on the substrate type, use of catalysts such as the PTAS, and precursor type (powder, gas). The most commonly used substrate for MoS_2 growth is the Si/SiO_2 substrate. Growth of up to centimeter scale MoS_2 on the Si/SiO_2 substrate has been reported [22]. MoS_2 growth on the SiO_2 layer, however, results in a massive amount of grain boundaries due to its non-epitaxial nature (Figure 1.6).

To eliminate the grain boundaries and obtain single-crystal monolayer MoS_2 without line defects, researchers have explored growth on single crystal substrates such as sapphire and GaN [23, 24]. As shown in Figure 1.7, there have been reports on epitaxial growth of MoS_2 on crystalline substrates. On the sapphire substrate, 91.5% of the MoS_2 showed alignment with the rest being aligned in other orientations. Continuous MoS_2 monolayer film up to the centimeter scale was achieved. However, due to 8.5% of the MoS_2 triangles not being aligned, the film results in high density of grain boundaries. On the GaN substrate, MoS_2 triangles show perfect

alignment. Thus, if these MoS_2 triangles merge to form a continuous film, no grain boundaries are expected to form. However, growing a large-scale continuous MoS_2 film using their method was not successful, which limits its application in the mass production of MoS_2 based devices.

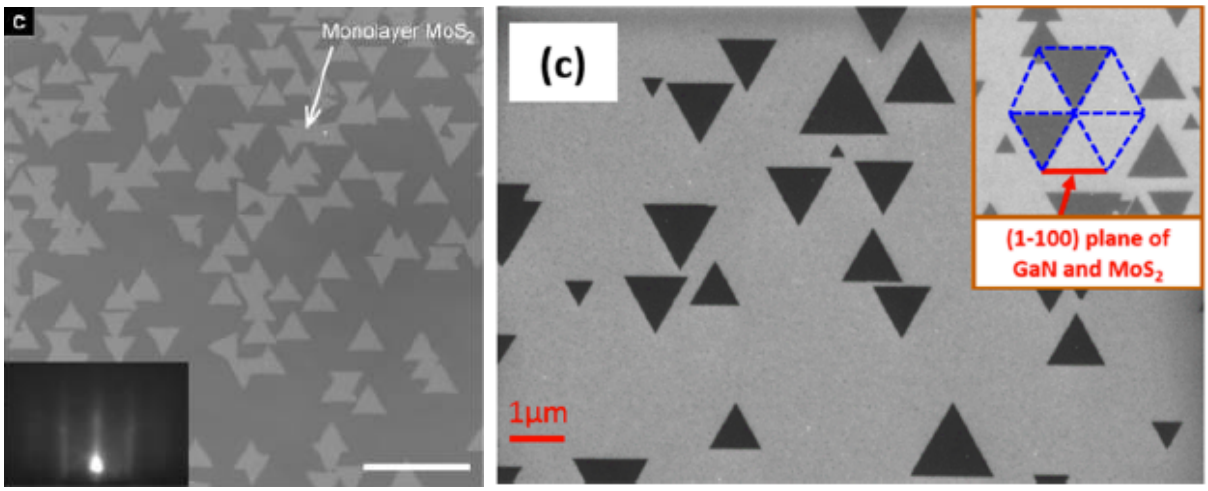

Figure 1.7 SEM images showing epitaxial growth of the MoS_2 monolayer on sapphire substrate (Left) and GaN substrate (Right). Adapted with permission from Reference [23]. Copyright (2015) American Chemical Society. Adapted with permission from Reference [24]. Copyright (2016) American Chemical Society.

To date, the most successful growth of large-area MoS_2 was done by using the MOCVD method. Kang et al. have achieved wafer-scale homogeneous MoS_2 monolayer films by using $Mo(CO)_6$ and $(C_2H_5)_2S$ gas as precursors [21]. The MoS_2 layer grown by the method showed uniformity throughout the entire 4-inch wafer. This is the first and only report on the wafer-scale homogeneous growth of the MoS_2 monolayer. This method, however, also results in very high density of grain boundaries in which most of the grain size is below 1 μm. Reports show that these grain boundaries in MoS_2 monolayers affect the device performance tremendously, reducing its conductance by down to 80% [25]. Thus, even with recent progress on the growth of

high-quality MoS_2 films, an improved method for growing large-scale single crystal MoS_2 is still needed.

CHAPTER 2 – GROWTH AND CHARACTERIZATION OF THE NANOWIRES

2.1 Defects in VLS Grown Nanowires

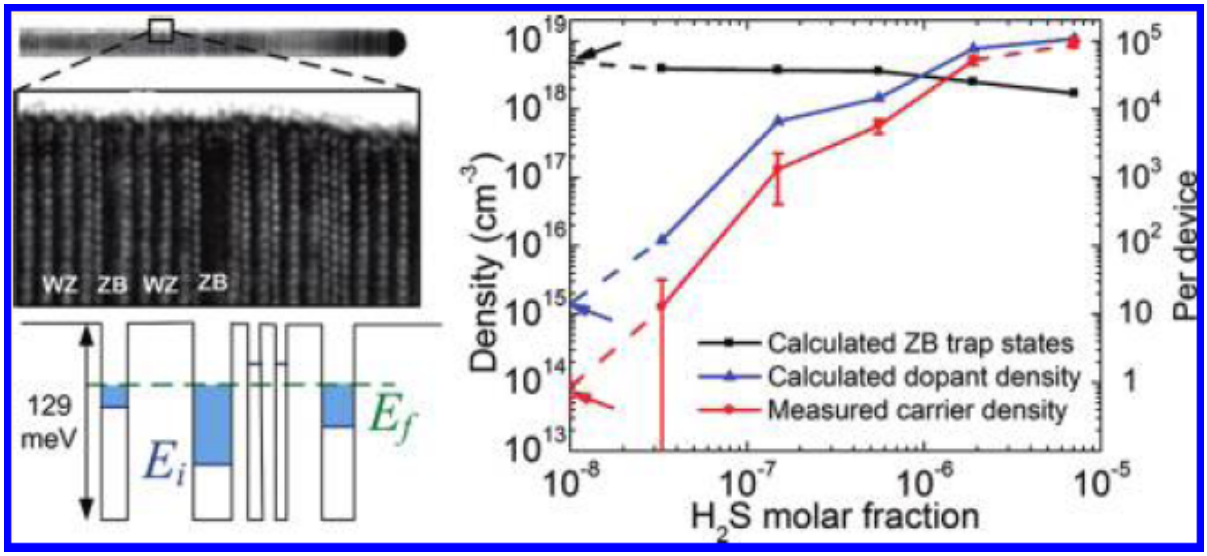

Figure 2.1 High-resolution TEM image of InP nanowires with stacking faults and a plot showing a difference between measured and calculated dopant density in the nanowire. Adapted with permission from Reference [26]. Copyright (2012) American Chemical Society.

Having full control of the nanowire geometry and the crystal structure is essential since they are closely related to the performance of the devices. For example, stacking faults occur very commonly in nanowire growths and it has been reported that for InP nanowires with stacking faults, up to ~5 X 10^{18}/cm^3 electrons can be trapped inside the local quantum wells formed by the band offset between zinc blende and wurtzite segments of the nanowire [26]. They show that the conductivity can be degraded down to an order due to the stacking faults as shown in Figure 2.1. For transistor applications, such defects in the nanowires are critical in the device performance and hence should be eliminated.

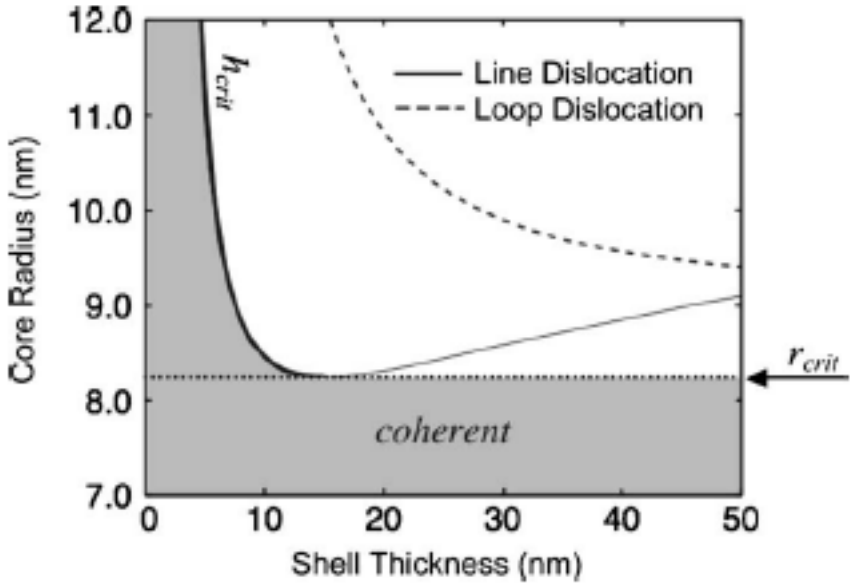

Figure 2.2 Plot showing calculated values for the critical thickness for the dislocation appearance. It can be seen that there is a region where the shell stays completely coherent with the nanowire regardless of the shell thickness. Reprinted from Reference [27] with the permission of AIP Publishing.

Unlike in thin films, stacking faults are the most common defects that occur in VLS-grown nanowires and dislocations are seldom observed in single-material nanowires. As mentioned previously, eliminating stacking faults is important in obtaining high-quality nanowires, and there have been several reports in the literature on growing completely stacking-fault-free nanowires [28, 29]. For core-shell nanowires, the shell behaves similar to thin films on wafers, and dislocations appear beyond a critical thickness of the shell. However, in conventional semiconductors, theory presumes an infinite dimension for the substrate thickness, thus the stress applied by the thin film on the substrate can be ignored, but in core/shell nanowires, the core and the shell has similar dimensions, and thus the stress applied by the shell on the core needs to be considered. This results in different critical thickness values for the shell which is dependent on the core diameters. Also, a critical core thickness exists (Figure 2.2) under which dislocation

does not appear regardless of the shell thickness [27, 30, 31], which does not exist in the wafer/thin film cases.

2.2 Growth and Characterization of Ultrathin III-V Nanowires for Transistors

Within the next ten years or so, it is expected that the transistors will reach sub-10 nm node and thus, researchers have suggested various materials for replacing silicon technology [32]. III-V nanowires, with more than an order higher electron mobility compared to silicon, is an excellent candidate for the new generation of transistors. Sub-10 nm III-V nanowires will be required for replacing silicon technology since in order to effectively suppress the short channel effects, body thickness needs to be smaller than the gate [33].

Figure 2.3 shows scanning electron microscopy (SEM) and the high-resolution transmission electron microscopy (HRTEM) images of ultrathin InAs nanowires [34]. The nanowires in the study were grown in a metalorganic chemical vapor deposition (MOCVD) chamber using the VLS method using Au nanoparticles. It can be seen that although ~50 nm diameter Au nanoparticles were used for the growth, smaller nanowires have grown within several micron distances from the original Au nanoparticles. It was demonstrated in [34] that the ultrathin InAs nanowires were grown from smaller Au nanoparticles that have formed by diffusing out of larger Au nanoparticles on the indium-rich surfaces during the nanowire growth. The ultrathin InAs nanowires do not have to be grown using larger Au nanoparticles, but can be grown using small diameter catalysts as well. The growth condition of the ultrathin InAs nanowires grown by using smaller catalysts is the same as in the case for using larger Au nanoparticles. It can be seen in the SEM images that there is a finite V/III ratio window for the ultrathin InAs nanowires to grow

and outside the window, only the larger nanowires grow. The average diameter of the ultrathin InAs nanowires were ~5 nm and down to ~2 nm diameter nanowires have been observed.

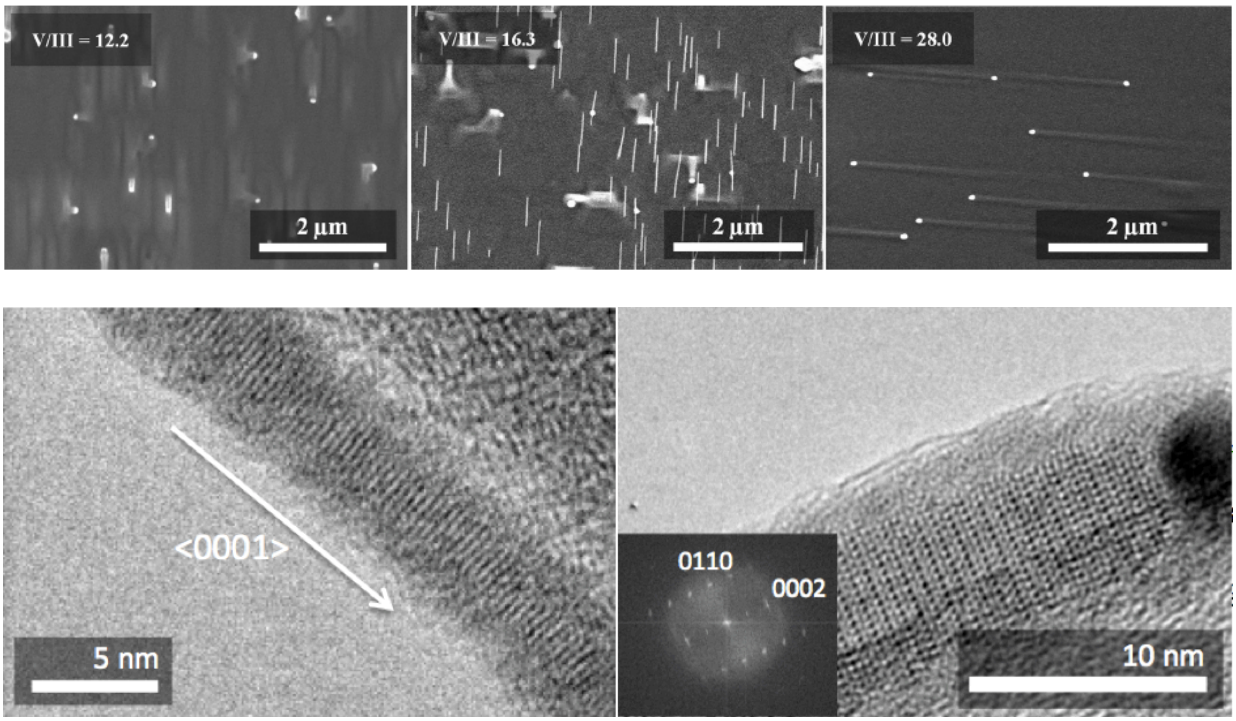

Figure 2.3 (Top) SEM images of ultrathin InAs nanowires showing V/III ratio dependence of the nanowire growth. (Bottom) HRTEM images of the as-grown ultrathin InAs nanowires. The zone axis is <2 -1 -1 0>.

HRTEM and the fast Fourier transform (FFT) images of the ultrathin InAs nanowires show that the crystal structure is wurtzite and the growth direction is <0001>. As shown in the Figure 2.3, the ultrathin InAs nanowires were completely stacking-fault-free with uniform diameters whereas the diameter variation between the base and the tip of the nanowire was less than 1 nm. With ~5 nm uniform diameter and defect-free/atomically smooth surface crystal structures, ultrathin InAs nanowires are excellent candidates for the short channel transistor applications.

2.3 Control of Au Atom Diffusion on Indium Rich Surface

As shown in Figure 2.3, under certain conditions, Au atom diffusion occurs during the nanowire growths, resulting in bimodal distribution of the InAs nanowires. An observation of the bimodal size distribution of the nanowire growth has been reported by Dailey and Drucker [35]. The authors claimed that upon hydrogen introduction into the growth chamber, the monolayer Au film that has been formed prior to the growth de-wet the surface to form ~15 nm Au particles. The Au particles grow into smaller NW along with the large NWs seeded from original Au particles. The InAs nanowires in Figure 2.3 were grown using Au colloids and no Au film was present between the colloidal particles to form the smaller nanowires.

Hertog et al. and Madras et al. have reported on the observation of Au atom surface diffusion occurring during silicon NW growth [36, 37]. Madras observed through in-situ TEM that Au can diffuse to the NW sidewalls in the form of AuSi under certain conditions and can separate from the thin AuSi liquid layer to form 3-5 nm Au particles during the cool down of the growth chamber. In our case, however, we observe that the ultra-thin InAs NWs grow out of the smaller Au particles which is a clear evidence that the smaller Au particle forms prior to the thinner NW growth, and not during the cool down of the growth chamber. We hypothesize that the onset of Au diffusion forming the ultra-small particles that seed NW growth results from the combination of InAs growth onset, Au splitting, and the appropriate growth condition.

To examine at which point the ultra-small Au particles are formed, two sets of experiments were carried out. First, we held the InAs substrates with 250 nm Au particles deposited at the growth temperature under 200 mbar with H_2 and As overpressure for 15 minutes prior to the initiation of the InAs NW growth. If it is energetically favorable for the large Au particles to spread out and form smaller Au particles before TMIn introduction, then the longer incubation

time should lead to the ultra-thin InAs NWs forming further away from the 250 nm Au particles or lead to higher ultra-thin InAs NW density. We have determined that holding the temperature does not change the maximum ultra-thin InAs NW growth distance from the originally deposited larger seeds nor their density, as compared to those without the temperature hold. Second, there is a possibility that the Au atoms diffuse out of the larger Au particles during the NW growth as previously observed by Hannon [38]. To examine the validity of this case in relation to the current study, we extended the NW growth time by a factor of 10 to establish whether there is a size reduction in the larger Au particles. The growth conditions were the same as the NWs in Figure 2.3, except for the increased growth time. We find that there is no size reduction of the Au particles during the NW growth. Thus, we conclude that the formation of the 5 nm Au particles occurs after the TMIn introduction into the chamber, but stops once the larger Au particles supersaturate and nucleate to form NWs. The fact that neither the ultra-thin InAs NWs nor the sub-10 nm Au particles could be observed on the sidewall of the larger NWs further supports our claim that Au atom diffusion is terminated once the Au catalysts are fully saturated with In.

From the experimental observations above, we can establish that two conditions must be satisfied in order for the Au atoms to diffuse out of the larger Au catalysts to form smaller Au particles: (i) a relatively high level of TMIn must be introduced into the system (i.e. low V/III ratio), and (ii) Au catalysts should not be fully saturated with indium. Condition (ii) implies that the Gibbs energy of mixing affects the Au atom diffusion process. Gibbs energy of mixing in the binary Au-In system has been reported by several groups. It was shown that the normalized Gibbs free energy of mixing (GM/RT), under the condition similar to our NW growth system, has a minimum value of almost -3 at 45.5% indium composition (Figure 2.4) [39], which

indicates that the alloying of Au and In lowers the energy of the catalyst significantly. Also, the Au and In alloy is known to show extremely rapid inter-diffusion [40].

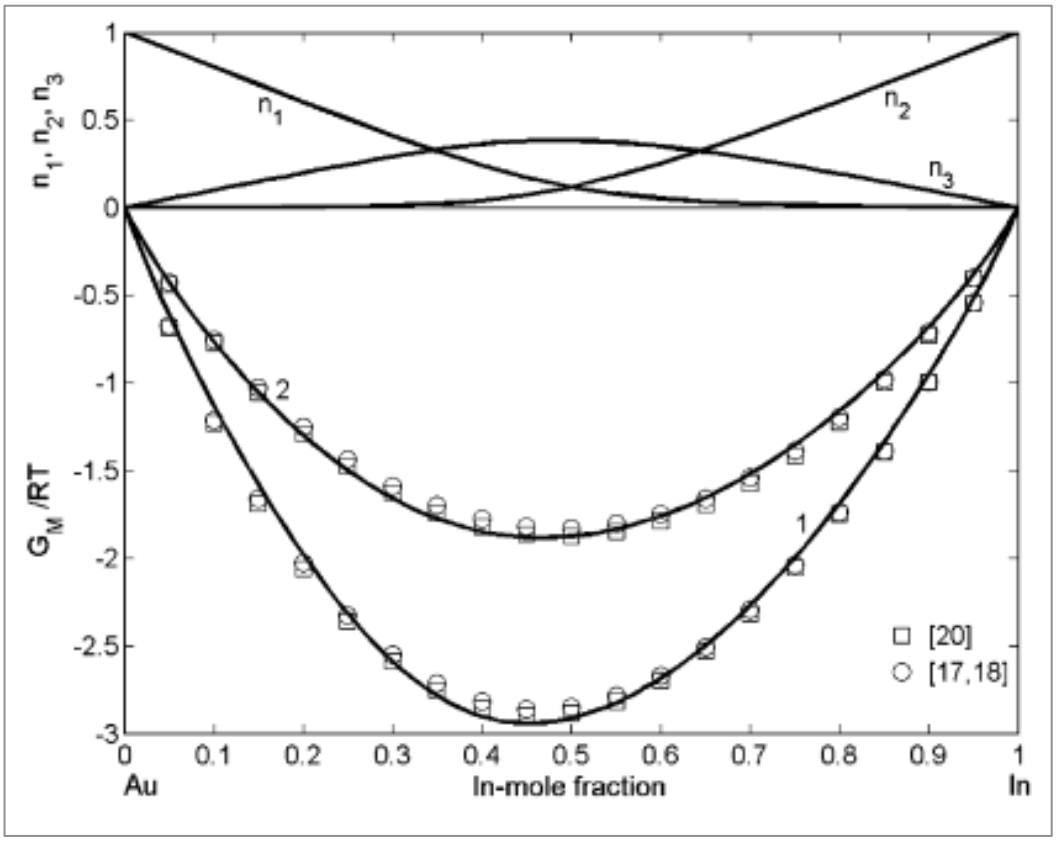

Figure 2.4 Gibbs energy of mixing as a function of indium-gold ratio. Reprinted from Ref [39], Copyright (2006), with permission from Elsevier.

Combining the factors noted above, we believe that diffusion of Au atoms occurs via the following process: The introduction of high TMIn flow into the growth chamber provides an indium-rich environment on the InAs surface. Au nanoparticles start to form alloys with In, thus, forming Au-In droplets. However, during the incubation period, a Gibbs free energy lowering from the intermixing of Au and In, combined with the local Au gradient, acts as a driving force for Au atom diffusing into the In-rich surface, forming an In-rich Au-In film within several micron distance from the original Au seeds. Au atoms then continue to diffuse out from the

catalyst as long as the energy lowering from the Au-In alloying and the diffusion driving force from the Au concentration gradient is larger than the surface tension increase from the catalyst curvature decrease. Thus, when the Au catalyst reaches a certain In saturation level, the diffusion of the Au atoms will stop. Au atoms that have diffused out will accommodate the growth of ultra-thin NWs once they reach the critical size to overcome the Gibbs-Thomson effect.

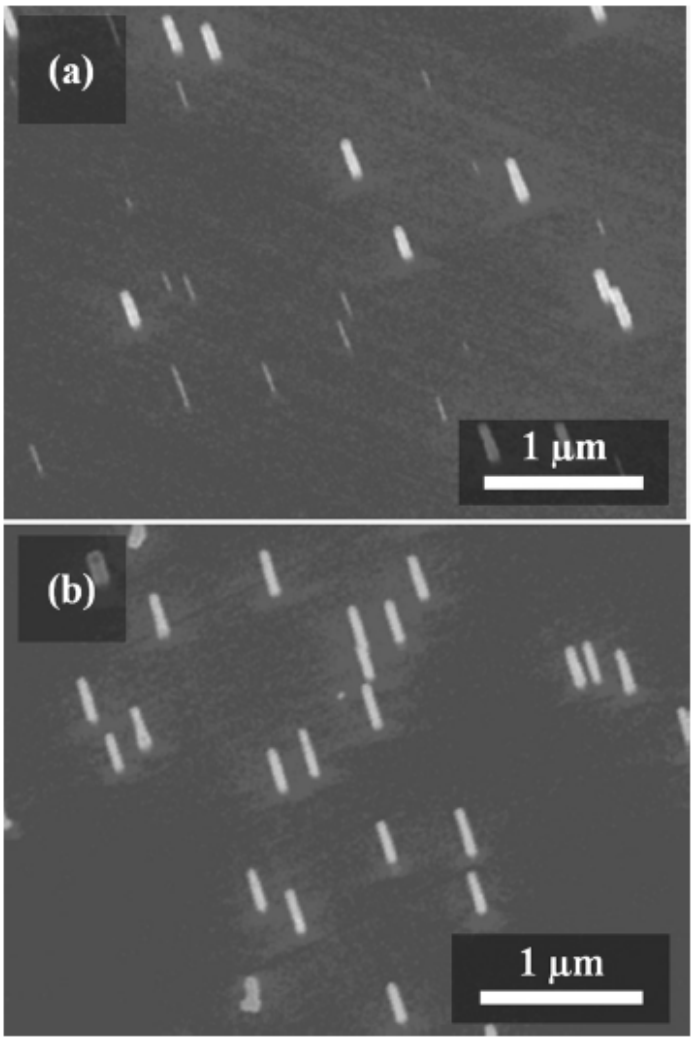

Figure 2.5 (a) An SEM image showing bimodal growth of nanowires. (b) An SEM image of nanowires grown using two-step growth. Notice that ultrathin InAs nanowires do not grow.

To further support our Au atom spreading mechanism, we have carried out a two-step InAs NW growth in which NWs were grown first in a high V/III ratio and then under typical bimodal growth conditions. The purpose of the first growth step in a high V/III ratio is to prevent Au atom diffusion during the incubation period of the Au nanoparticles. Figure 2.5 shows a comparison of InAs NWs grown on InAs (110) substrates using 50 nm Au nanoparticles with and without this high V/III ratio incubation period. The InAs NWs in Figure 2.5(a) were grown under the typical bimodal growth conditions (450 °C, V/III = 9.8) for 3 minutes, whereas in Figure 2.5(b), the sample was held in a V/III ratio of 28 for 10 minutes, followed by 3 minutes of growth under the same conditions as the sample in Figure 2.5(a). Indeed, the high V/III ratio incubation period has effectively inhibited the diffusion of the Au atoms on the wafer surface. Thus, it can be seen that the control of Au atom diffusion during the nanowire growth can be controlled to obtain nanowires with the desired size.

2.4 Core/Shell Nanowire Growth and Characterization

Transistors based on core/shell nanowire structures have intrigued many researchers since they are known to reduce the carrier scattering at the nanowire surface resulting in enhanced mobility [3]. Also, core/shell heterostructured nanowires are excellent candidates for devices such as tunnel field-effect transistors and high-electron-mobility transistors (HEMT) [41, 42].

Figure 2.6 shows two types of core/shell nanowires grown using ultrathin InAs nanowires as a core. The left image shows InAs/AlAs core/shell nanowires with ~5 nm core and ~5 nm AlAs shell and the right image shows InAs/AlAs/GaAs core/multishell nanowires with 5 nm InAs core and 4 nm/2 nm AlAs/GaAs shells. Because the AlAs layer oxidizes rapidly in the atmosphere, AlAs shells in the InAs/AlAs core/shell nanowires oxidize into aluminum oxide as soon as they

are taken out of the MOCVD growth chamber. For InAs/AlAs/GaAs core/multishell nanowires, the outermost GaAs layer protects the AlAs layer from oxidation and thus the AlAs layer maintains its crystallinity.

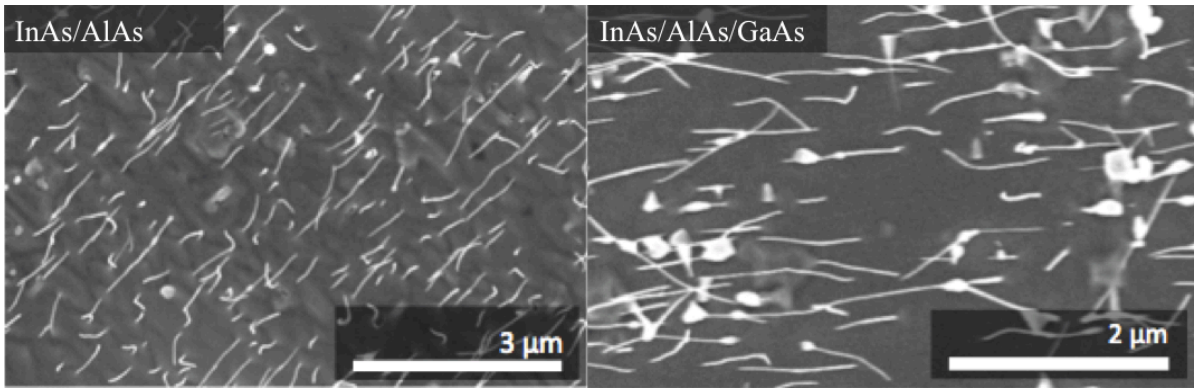

Figure 2.6 SEM images showing InAs/AlAs core shell nanowires and InAs/AlAs/GaAs core/multishell nanowires.

The TEM image of the InAs/AlAs core/shell nanowires shows that the InAs core has been deformed significantly from the oxidation of the shell. It can be seen that even with extreme deformation of the core, the nanowire has not been broken, showing its mechanical flexibility. The fact that the ultrathin InAs nanowires can be bent up to ~90˚ without breaking, will be utilized to form nanowire arrays which will be explained in Chapter 3.

The HRTEM image of the InAs/AlAs/GaAs core/multishell nanowires shows clear edge dislocation formation at the InAs/AlAs interface. Although Raychaudhuri et al. have predicted the presence of a critical core diameter beneath which no dislocations can be formed regardless of the shell thickness [27], we could not observe the completely coherent core/shell nanowire structures with the core diameters we have studied which is probably due to the large lattice mismatch between the InAs and the AlAs.

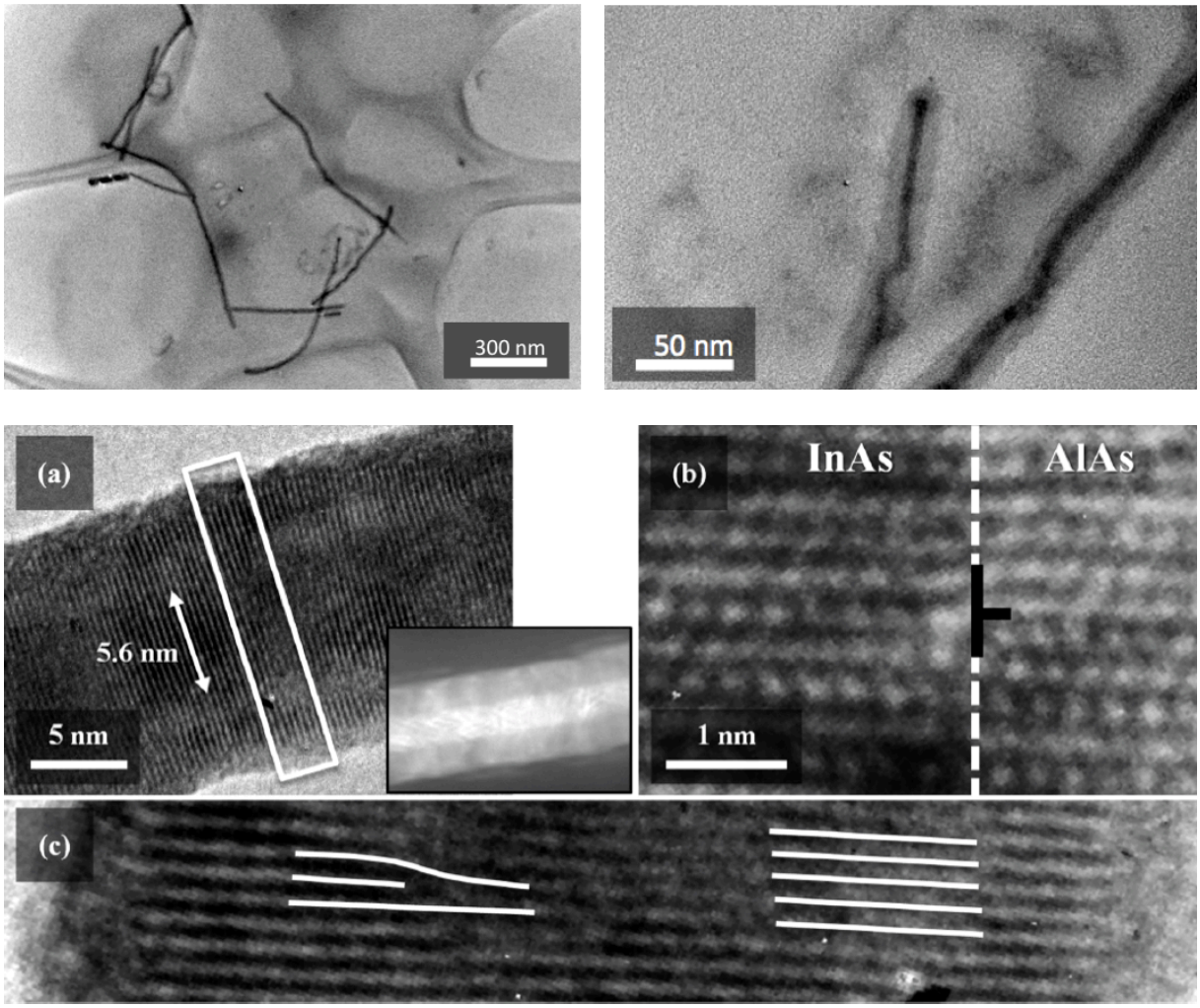

Figure 2.7 HRTEM images of InAs/AlAs core shell nanowires and InAs/AlAs/GaAs core/multishell nanowires. Clear edge dislocations can be seen in the InAs/AlAs/GaAs core/multishell nanowires at the InAs/AlAs interface.

One interesting observation is that although the crystal structure of the InAs core was wurtzite, nonmatching dislocations on each side of the nanowires could be observed as shown in Figure 2.7. Similar nonmatching dislocations have been reported previously by Dayeh et al. for the Ge/Si core/shell nanowires [43], but the structure of Ge/Si nanowires are diamond cubic and thus edge dislocations can be formed in a slanted fashion. However, for InAs/AlAs/GaAs nanowires, the core and the shell are comprised of wurtzite crystal structures, and because slip planes for the dislocations can only be parallel or perpendicular to the <0001> directions, slanted

dislocations cannot be formed. Further study will be needed to completely understand the nonmatching edge dislocations in the wurtzite core/shell nanowires.

The HRTEM image of the edge dislocations clearly shows the Frank type partial dislocation which forms a local zinc-blende type stacking in the shell. The degree of strain relaxation in the InAs/AlAs/GaAs can be calculated through the observation of edge dislocation frequency. It was found that the edge dislocations occur approximately every 20 atomic planes. This corresponds to ~ 5% strain relaxation which is much lower than the expected value coming from InAs/AlAs lattice mismatches. This shows that the strain relaxation in the axial direction of the nanowire is not complete and is only partially relaxed.

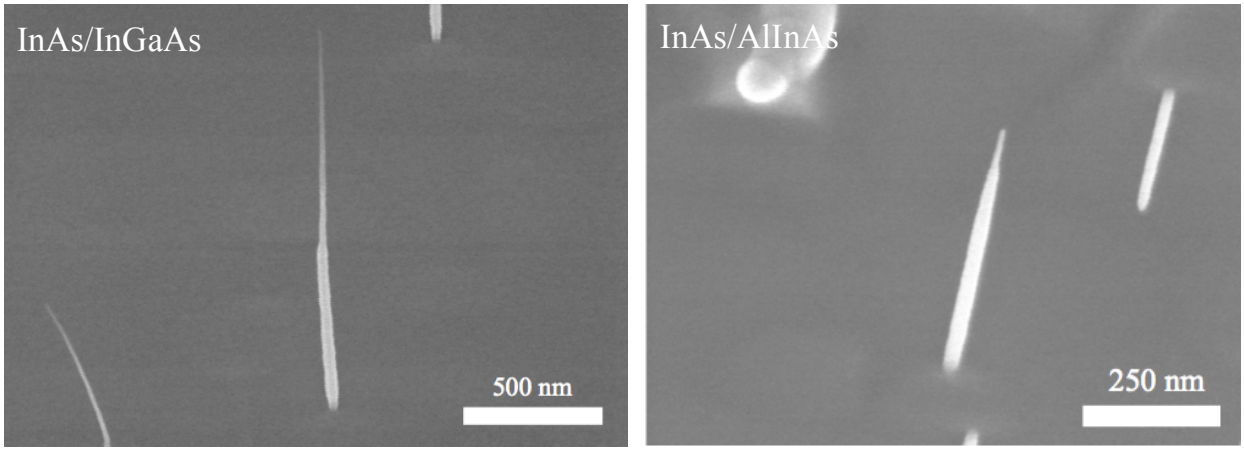

Figure 2.8 SEM images showing InAs/InGaAs and InAs/AlInAs core/shell nanowires with 5 nm diameter core.

Next we explore the structure of InAs/InGaAs and InAs/AlInAs core/shell nanowires. Unlike InAs/AlAs or InAs/AlAs/GaAs nanowires shown in Figure 2.6, InGaAs and AlInAs shells are better in terms of dislocation formation due to their capability of controlling the composition. Figure 2.8 shows SEM images of the core/shell nanowires. We aimed for growing 50% indium in InGaAs shells and 67% indium in AlInAs shells. Because the TMGa cracking

rate is much lower than TMIn at the growth temperature (450 ˚C), we flew TMGa four times the amount of TMIn. Also, to enable the lateral growth rather than the axial growth, large amount of arsine was flown for the shell growth.

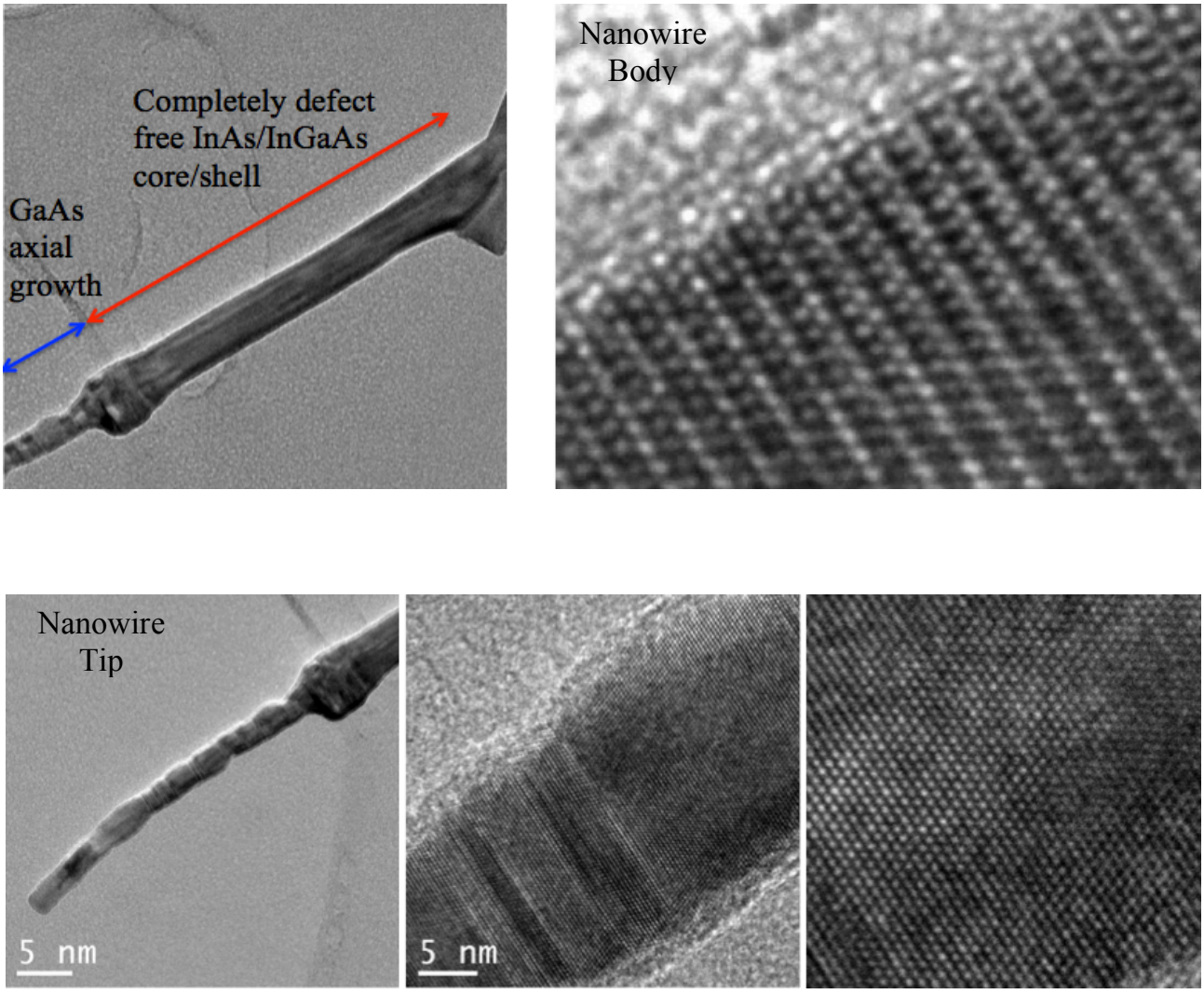

Figure 2.9 HRTEM image of InAs/InGaAs core/shell nanowires. The crystal structure of the nanowire body is wurtzite whereas the crystal structure of the tip is zinc blende. GaAs axial growth occurs during the InGaAs radial growth on the InAs nanowires.

Figure 2.9 shows HRTEM images of InAs/InGaAs nanowires. The InGaAs shell is 15 nm thick on each side of the InAs core. It can be seen that there is both radial and lateral growth. The

nanowire body has an InAs core and an InGaAs shell with 50% indium composition. The crystal structure is wurtzite with no stacking faults in the entire body region. Also, no sign of dislocation can be seen. Lattice constant is measured to be 6.772 Å in the c-axis (growth direction) which matches the composition. The fact that no dislocations were observed but the lattice constant of the shell matched the EDX implies that the core may be under compressive stress.

On the other hand, the tip part shows a large number of stacking faults. Also, the crystal structure is ZB whereas the InGaAs grown over the InAs core was WZ. No EDX was done but the inter-plane distance in the (111)B direction was measured to be 3.26 Å implying that the axial growth part is pure GaAs.

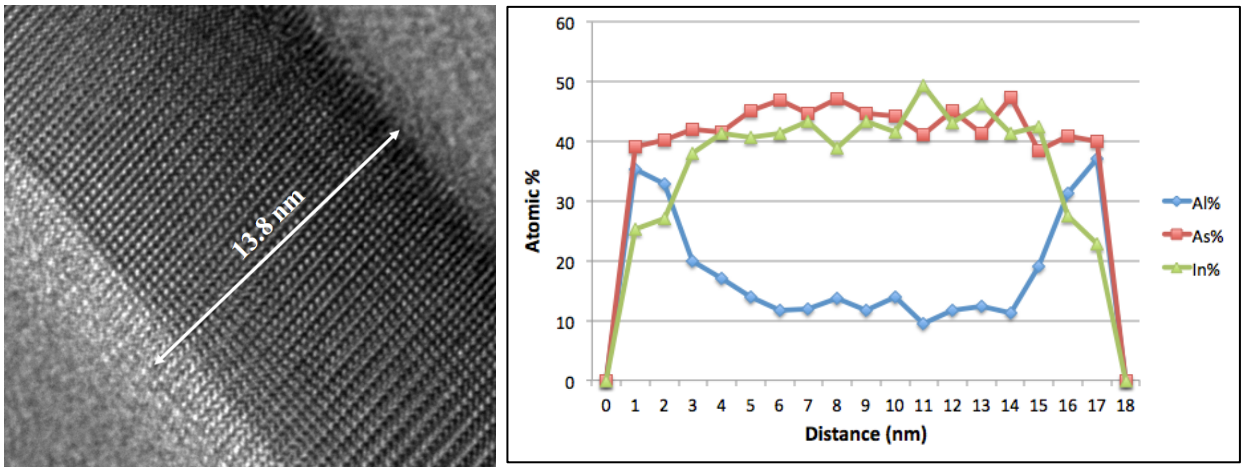

Figure 2.10 (Left) HRTEM image of an InAs/AlInAs core/shell nanowire. (Right) EDX data measured along the radial direction of an InAs/AlInAs nanowire.

The HRTEM analysis was done on the InAs/AlInAs core/shell nanowires as well. Figure 2.10 shows a lattice resolved TEM image, EDX analysis, and bright-field/HAADF image showing the contrast between the core and the shell. The HRTEM image shows that the nanowire is a wurtzite structure, and the EDX composition analysis shows that the shell is 67%

indium and 33% aluminum. The diameter was uniform, and the thickness variation from the base to the top of the core/shell part was less than 2 nm.

Thus, we have shown various types of core/shell nanowire growths. By optimization of the V/III ratio and the temperature, stacking-fault-free core/shell nanowires could be grown. Also, for the InGaAs shell and the AlInAs shell nanowires with certain compositions, we could not find any dislocations although the mismatch between the core and the shell is relatively large, which shows the possibility of the InAs core being below the critical limit for dislocation formation.

2.5 Growth of Defect-Free InAs Nanowires and Axial Heterostructured Nanowires

As mentioned in Chapter 1, growth of defect-free nanowire structures is critical in obtaining high-performance devices because carriers are known to get trapped or scattered at stacking faults [26]. For III-V nanowires, stacking faults occur frequently, and thus it is hard to obtain completely stacking-fault-free nanowires compared to group IV based nanowires. Only a few groups have achieved stacking-fault-free III-V nanowires [28, 29]. The most common approach for obtaining stacking-fault-free nanowire is through two-step growth [29].

We have achieved stacking fault InAs nanowires through just tuning the V/III ratio and temperature. Figure 2.11 shows a HRTEM image of a completely stacking-fault-free wurtzite phase InAs nanowire. The nanowire was grown at 450 ˚C with a V/III ratio of 10.3. We find that the V/III ratio window for obtaining stacking-fault-free InAs nanowire is small, and less than 5% change in the V/III ratio results in a massive amount of stacking faults within the nanowires.

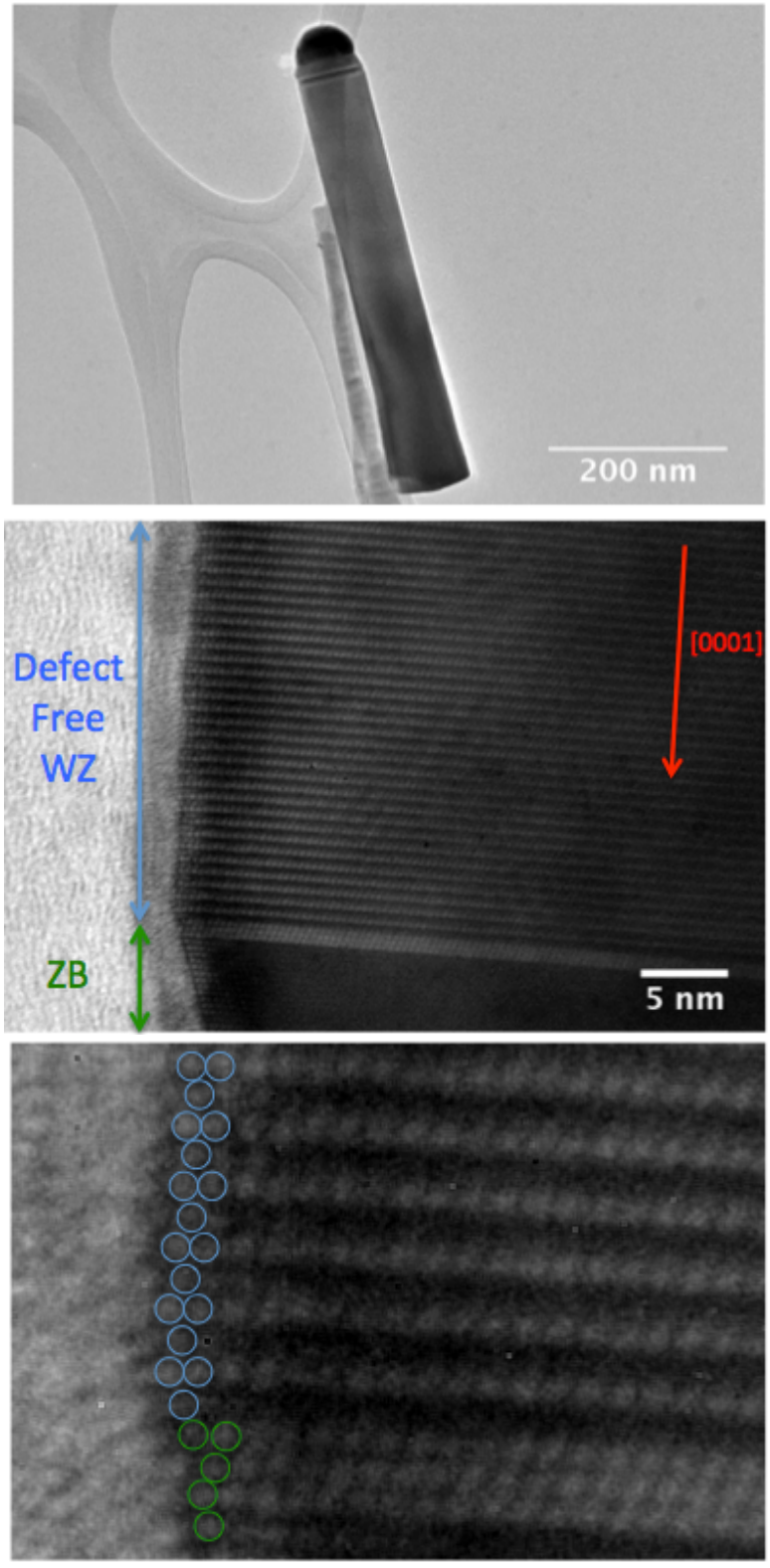

Figure 2.11 HRTEM of stacking-fault-free InAs nanowire with wurtzite crystal structure. The entire nanowire was wurtzite phase except near the tip where it showed zinc blende phase.

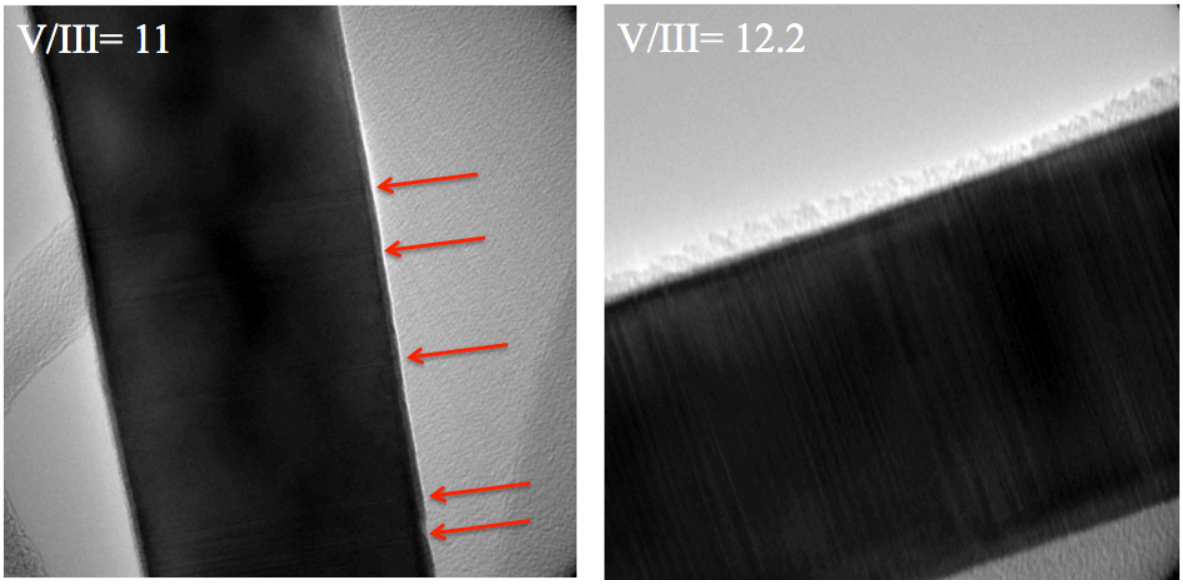

Figure 2.12 HRTEM of InAs nanowires grown at different V/III ratios. Red arrow indicates the position of the stacking faults.

Figure 2.12 shows the HRTEM of InAs nanowires grown at different V/III ratios. It can be clearly seen that as the growth condition shifts out of optimal stacking-fault-free V/III ratio window, a multiple crystal phase starts to appear. At V/III=11, the InAs nanowire showed a stacking fault density of ~2 stacking faults/100 nm. But at V/III = 12.2, the InAs nanowire turned into a completely polytypic phase with random alternation of wurtzite and zinc blende crystal structures throughout the entire nanowire. Thus, it can be seen that the precise control of the growth condition is needed in order to obtain defect-free nanowires.

For certain applications such as tunnel FETs [41], it is desirable to grow axial hetero-structures. We have grown GaAs-InAs and GaAs-InAs-GaAs heterostructure nanowires. Figure 2.13 shows SEM images of the nanowires. For both types of nanowires, the GaAs base segment has been grown for 60 s. It can be clearly seen that the InAs axial segment starts to grow along with the InAs deposition on the GaAs surface.

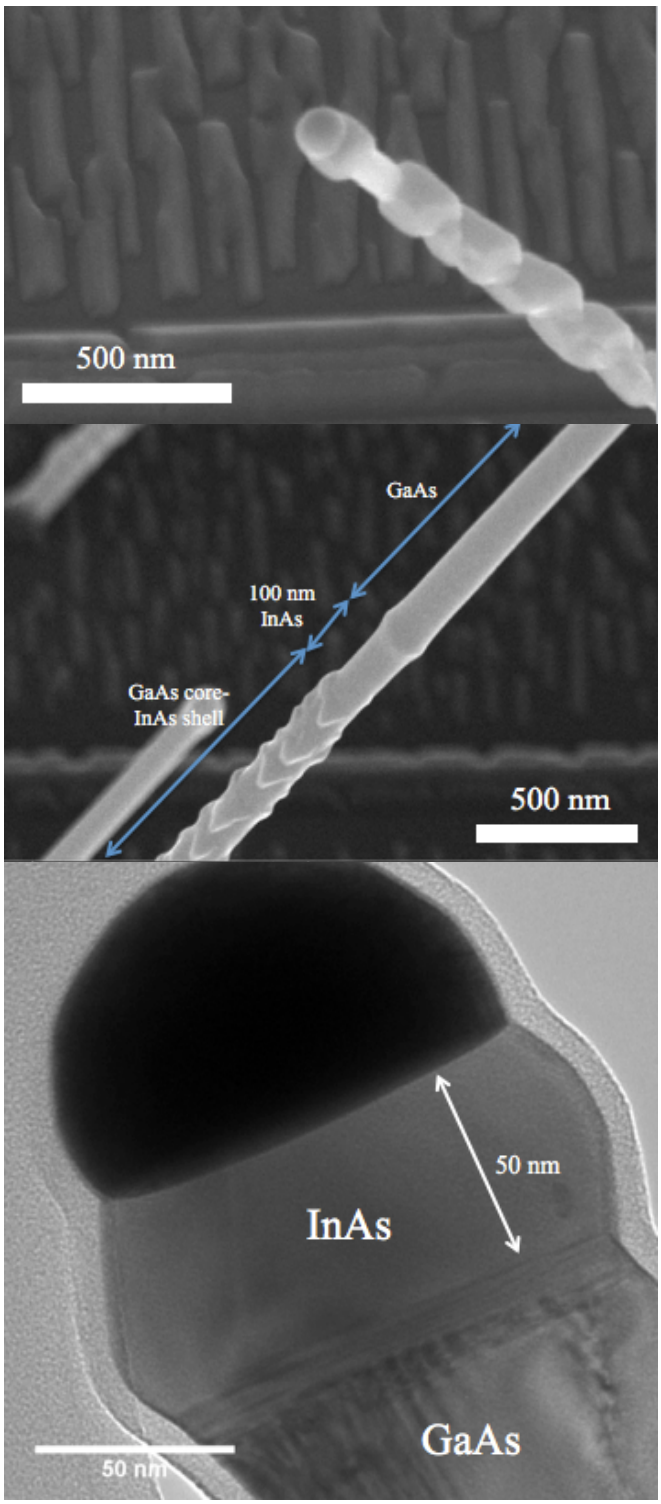

Figure 2.13 (Top) GaAs-InAs axial heterostructure nanowire. (Middle) GaAs-InAs-GaAs axial heterostructure nanowire. (Bottom) TEM image showing the interface between InAs and GaAs in a GaAs-InAs nanowire.

For GaAs-InAs-GaAs nanowires, three segments can be clearly seen. The first GaAs segment is very rough due to the InAs deposition on the nanowire surface. The InAs segment and the second GaAs segment have a smooth surface. Interestingly, the InAs deposition on the GaAs surface forms as islands whereas the GaAs deposition on the InAs surface forms as a continuous film. Another interesting observation is that although the V/III ratio of the GaAs and InAs segment growth conditions are similar, the growth rate is very different. The GaAs segment grew at a rate of ~35 nm/s whereas InAs segment grew at a rate of 0.28 nm/s. This may be due to the tendency of indium to stay within the Au catalysts [44].

CHAPTER 3 – ELASTOCAPILLARY-FORCE-INDUCED LARGE-SCALE ALIGNMENT OF VLS GROWN NANOWIRES

As mentioned in the previous sections, the absence of a method for aligning VLS grown nanowires in a large scale acts as one of the biggest barriers for the nanowires to be used in commercial products. In this section, the elastocapillary-force-induced large-scale nanowire alignment method will be proposed. The elastocapillary-force alignment resulted in a record high yield as well as more than an order improvement in the density of the nanowires.

3.1 Elastocapillary-Force-Induced Nanowire Alignment

Figure 3.1 shows the elastocapillary-force-induced nanowire alignment process and the SEM images of before/after the alignment with various substrate/nanowire combinations. The elastocapillary-force alignment process has a great advantage in terms of simplicity in the method and the fact that the method does not require any complex setup. Elstocapillary-force alignment was done through growing nanowires at a tilted angle followed by dipping the entire sample into DI water and drying with nitrogen gun. We observe that the tilted nanowires always bend down onto the projection of the nanowires on the substrate. Thus, on (100) zinc blende substrates, zinc blende or wurtzite nanowires grow into two (111)B directions and lie down into the projection resulting in planar alignment in two directions, and on (110) substrates, nanowires align in a single (111)B projected direction. We have also tested various nanowire/substrate material combinations in elastocapillary-force nanowire alignment such as GaAs nanowires on GaAs wafers, InAs nanowires on InAs wafers, and InAs nanowires on InP wafers. We find that the method can be applied to all of them. The dipping direction of the sample and the nitrogen gun blowing direction did not affect the nanowire alignment yield.

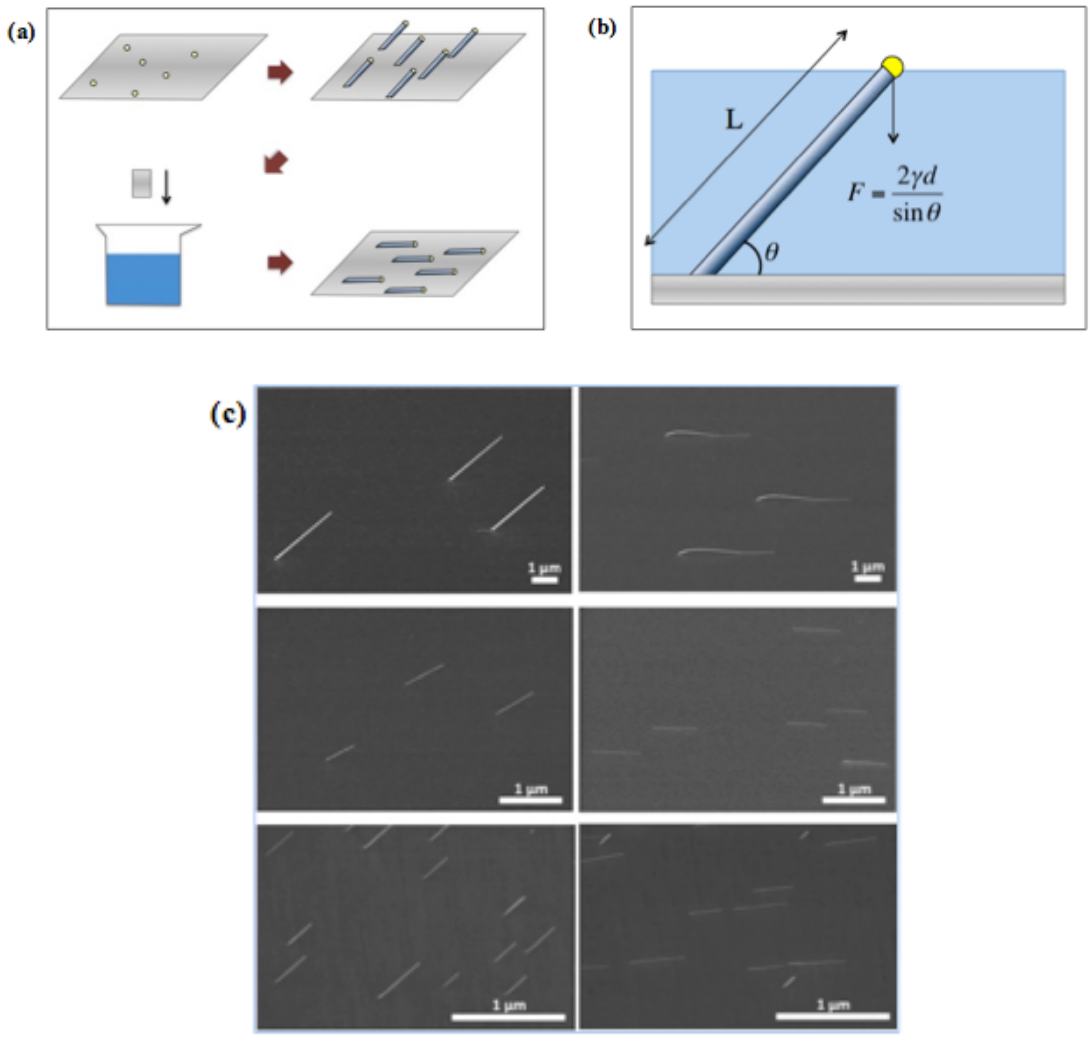

Figure 3.1 Nanowire aligning process. (a) Illustration of nanowire aligning process. Nanowires are grown at a tilted angle by the VLS method using Au nanoparticles. The entire substrate is then dipped into DI water briefly. Residual water droplets are blown away using nitrogen guns. The nanowires on the sample taken out of DI water are laid down into the projection on the substrate. (b) Illustration of elastocapillary-force acting on a nanowire upon drying of water. (c) 35˚ tilted SEM images showing nanowires before the alignment and after the alignment process. (Top) 30 nm diameter GaAs nanowires on GaAs(110) substrate. (Middle) 5 nm diameter InAs nanowires on InP(110) substrate, (Bottom) 5 nm diameter InAs nanowires on InAs(110) substrates. Note that for InAs nanowires on InAs substrates, shorter nanowires have not laid down due to the length being below the critical value.

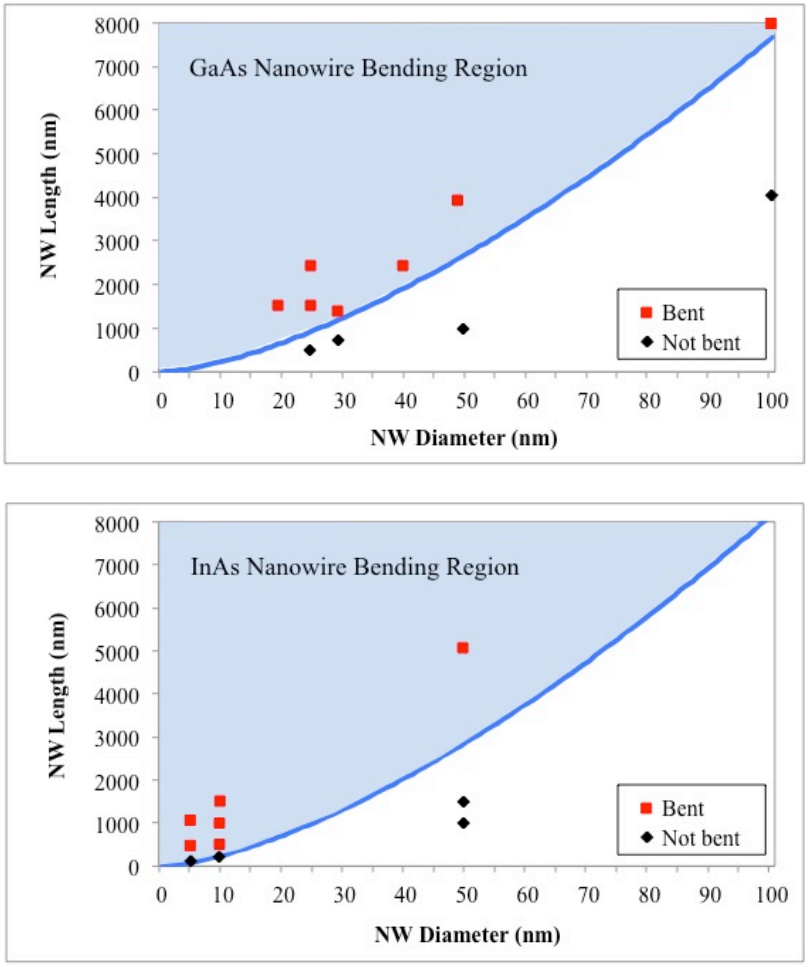

Figure 3.2 Plot of nanowire bending criteria under elastocapillary-force for InAs and GaAs nanowires. Red and black dots indicate bent and not bent nanowires observed experimentally.

A model of an elastic rod bending at a liquid surface has been well modeled by Neukirch et al. [45]. In the model, when the liquid level becomes lower and reaches the tip of the rod, the bending starts to occur due to capillary forces, and the force acting on the nanowires can be expressed as [45],

$$F = \frac{2\gamma d}{sin\theta} \tag{3.1}$$

where γ is the surface tension of the liquid, d is the diameter of the nanowire, and θ is the angle between the nanowire and the substrate. Thus, for typical 25 nm diameter and 2.5 µm long GaAs

nanowires grown on GaAs(110) used in this study, the capillary bending force the nanowire receives during the drying of the water will be ~4.4 X 10^{-9} N. Notice that the force the nanowire receives upon evaporation is independent of the nanowire length but is dependent on the nanowire diameter. However, the force required for the nanowires to bend down is a function of both the nanowire length and the diameter, and can be expressed as [45],

$$F_{bend} = \left(\frac{\pi}{2}\right)^2 \frac{EI}{L^2} \tag{3.2}$$

where the *E* is the young's modulus of the nanowire, *I* is the second area moment of the cross section of the nanowire, and *L* is the length of the nanowire. Assuming cylindrical GaAs nanowires with a 25 nm diameter and 2.5 μm length, the force required to bend the nanowires can be calculated as ~6.47 X 10^{-10} N. Note that this is a simplified calculation, and for more precise results, other forces such as van der Waals force between the nanowire and the substrate need to be taken into account. Also, although we used Young's modulus of bulk GaAs in the calculation, it has been reported that the Young's modulus of nano scale materials differs from its bulk values and is dependent on its diameter [46]. It can be seen in the equation that as the length of the nanowire decreases, more force is required to bend the nanowires, and we observe that there is a critical length (L_c) as a function of the nanowire diameter below which the nanowires do not bend down to the substrate. This can be clearly seen in Figure 3.1(c) for the InAs nanowire on InAs(110).

From Equation (3.1) and Equation (3.2), the criteria for the nanowires to bend down can be derived as a function of the diameter. Assuming the nanowires have a cylindrical cross section and the dipping solution is room-temperature water, the conditions for the nanowires to bend down can be shown as,

$$L(GaAs) \geq \sqrt{\frac{d^3}{1.7\times10^{-11}}}, \qquad L(InAs) \geq \sqrt{\frac{d^3}{1.5\times10^{-11}}} \tag{3.3}$$

The difference between the two equations comes from the difference in the Young's modulus between GaAs and InAs. The critical length of the nanowires for bending in water can thus be expressed as,

$$L_c(GaAs) = \sqrt{\frac{d^3}{1.7\times10^{-11}}}, \qquad L_c(InAs) = \sqrt{\frac{d^3}{1.5\times10^{-11}}} \tag{3.4}$$

From Equation (3.3), it can be seen that for thicker diameters, longer nanowires are required in order for them to lie down. For GaAs nanowires, ~1 μm length is needed for 25 nm diameter nanowires to bend down and ~2.8 μm length is needed for 50 nm diameter nanowires to bend down. Thus, controlling the diameter and the length of the nanowires is critical in order to achieve good yield in elastocapillary-force nanowire alignment. Figure 3.2 shows plots indicating the conditions for bending of GaAs and InAs nanowires. Within the blue region, the nanowires bend down onto the substrate whereas outside the blue region, the nanowires do not bend down. Experimental observation of the nanowire bending and none-bending conditions has been added to the plot in red and black dots.

3.2 Large-Scale Single-Nanowire Arrays by Elastocapillary-Force Nanowire Alignment

One remarkable thing about these nanowires is that even after they have been laid down, the base of the nanowire is still attached to the substrate as shown in Figure 3.1, which means that the initial position of the nanowire is unvaried. Thus, to achieve single nanowire planar arrays with precise positioning at a desirable place, e-beam patterned Au dots were used for the growth and alignment of nanowires. Thus, 75 X 15 X 6 Au dots (6750 dots in total) have been patterned over 1.6 cm X 1.2 cm GaAs substrate in order to demonstrate that large-scale planar

single-nanowire arrays can be achieved. Out of 6750 dots, 66 dots were missing probably due to lithography or lift off problems and 12 nanowires were grown in none (111)B directions. The rest of the nanowires that were grown in (111)B directions have all been aligned into the projection of the nanowire on the wafer surface with less than $\pm 5^{\circ}$ misalignment angles as shown in Figure 3.3. Thus, we have achieved 98.8% yield of single nanowire arrays including the missing Au dots and 99.8% yield without considering the lithographical error. Similar yield could be achieved for 25 nm diameter and 2.5 μm long GaAs nanowires when dipping the sample into acetone or methanol.

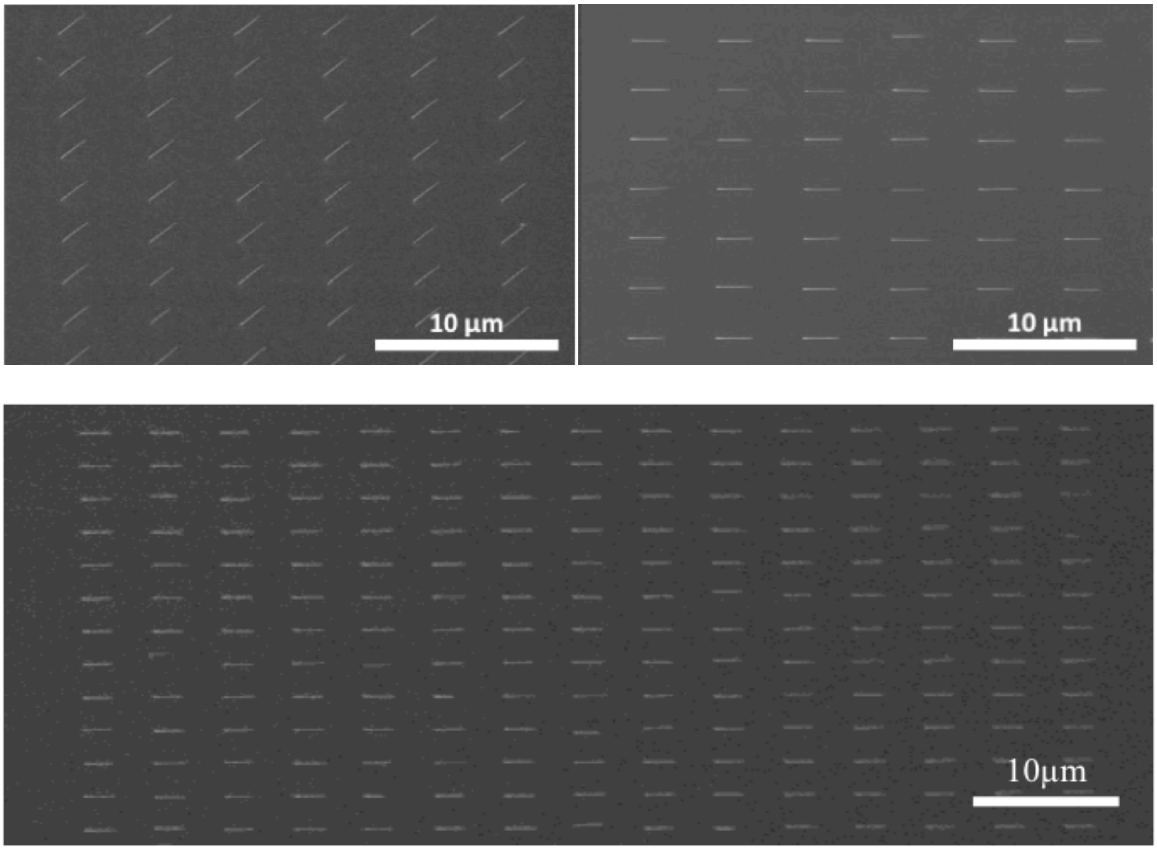

Figure 3.3 (Top) 30˚ tilted view of GaAs nanowires on GaAs substrates before and after dipping into water. (Bottom) top view of SEM image showing a lower magnification view of aligned nanowires.

There is also an attractive force acting between the nanowires upon drying of the solution, and controlling the adhesion between the nanowires is critical in obtaining planar single nanowire arrays without crossing defects. Figure 3.4 shows nanowire arrays formed with different pitches. The nanowires used in this study are GaAs nanowires grown on GaAs(110) with 2 - 2.5 μm in length and ~25 nm in diameter. Within 1 – 3 μm pitch the planar single nanowire array yield is over 97%, but beneath 1 μm pitch, the yield goes dramatically down and nanowires start to stick to each other to form crossing defects. For 300 nm pitch sample, almost all of the nanowires are attached to each other to form groups of 2 - 4 nanowires.

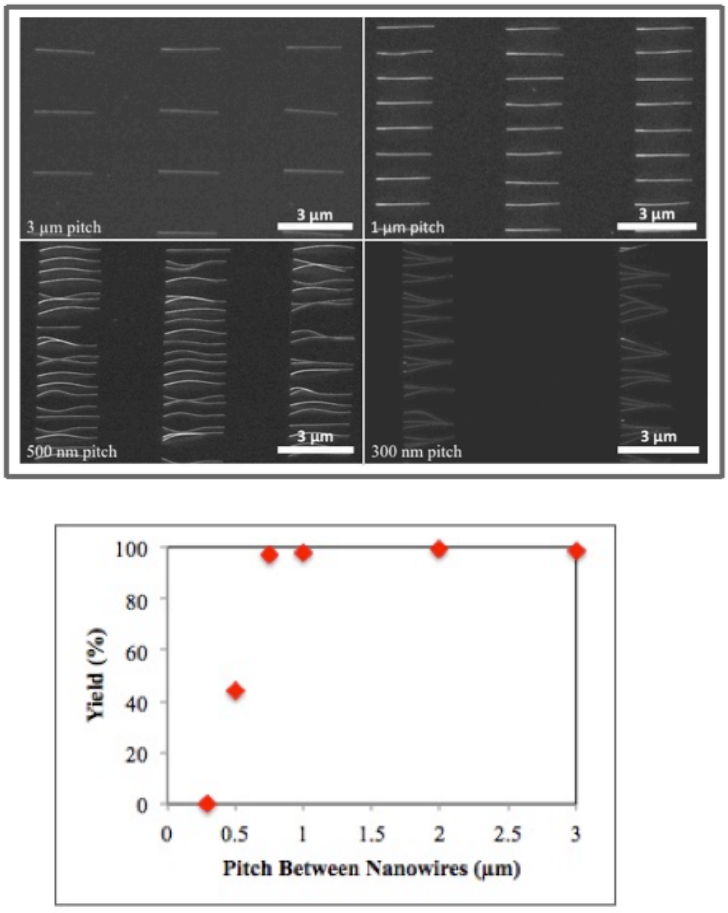

Figure 3.4 (Top) SEM images showing pitch dependence on the elastocapillary-force alignment of nanowires. (Bottom) Plot showing pitch dependence on the single nanowire alignment yield.

The force required for the nanowires to bend toward each other can also be expressed as Equation (3.2), but the force acting between the nanowires is immersion capillary force and thus differs from the force that bends the nanowires down to the substrate. Immersion capillary force has been well modeled by Kralchevsky et al. for the case of colloidal particles and can also be applied to nanowires as well [47]. During the elastocapillary-force nanowire alignment process, when the liquid level reaches the tip of the nanowire, the tip of the nanowire will be partially immersed in water. Due to the formation of meniscus, the nanowires will experience immersion capillary force between each other. By assuming that the immersion capillary force between the nanowires come only from the tip of the nanowires, the immersion capillary force acting between the nanowires can be expressed as,

$$F_i = a\frac{r^2}{l} \tag{3.5}$$

where r is the radius of the nanowire, l is the pitch between the nanowires, and a is a fitting parameter which is relevant with the surface tension of the liquid and the slope of the meniscus between the nanowires. As mentioned above, this is a simplified model and in the actual nanowire aligning process, as the nanowires bend down, immersion capillary force between the nanowires would increase. This is because at the early stage of nanowire bending, only the tip of the nanowire would be at the surface of the liquid, but as the liquid level gets lower and nanowire bends down, more of the nanowire would be at the surface of the liquid, leading to increased immersion capillary force. Thus, F_i would be a function of nanowire length as well. For 25 nm diameter and 2.5 μm long GaAs nanowires, the $F_{bend} = 6.47\times10^{-10}$ N, and since we observe experimentally that the adhesion between the nanowires occurs at approximately 800 nm pitch, a can be calculated as 3.31 and thus,

$$F_i(GaAs) = 3.31\frac{r^2}{l} \tag{3.6}$$

To achieve high-density planar single nanowire arrays without having crossing defects, F_{bend} has to be smaller than the elastocapillary-force but larger than the immersion capillary force, and thus, the $F_e > F_{bend} > F_i$ condition has to be met. Because it can be seen in Equation (3.5) that the immersion capillary force is independent of nanowire length, reducing the nanowire length would allow shorter pitch between the nanowires without having crossing defects since F_{bend} increases with the decrease of the nanowire length. The pitch between the nanowires can thus be controlled by designing the nanowire diameter and length. For example, to achieve single GaAs nanowire arrays with a 10 nm diameter and 200 nm pitch between the nanowires, the length of the nanowires has to be within 136.7 – 282.3 nm. If the length of the nanowire is shorter than the range, the nanowires would not lie down due to insufficient elastocapillary-force, and if the length of the nanowire is longer than the range, the nanowires would stick to each other to form crossing defects. Since shorter nanowires are required to minimize the crossing defect from immersion capillary force, and thinner diameter is needed to bend the nanowires down from the elastocapillary-force, higher density of single nanowire arrays can be achieved by using thinner and shorter nanowires.

3.3 Achieving Arrays of Multiple Nanowires per Site Using Elastocapillary-Force

For some nanowire-based applications, it is desirable to have multiple nanowires per site. For example, in order to fabricate nanowire-based CMOS using III-V nanowires, multiple p-type nanowires per site would balance the current in n-type nanowires since the electron mobility of most III-V nanowires is more than an order higher than the hole mobility. Increasing the diameter of the p-type nanowires would also increase the current in the nanowires but the

increased diameter would result in reduced gate control capability and thus would result in increased short channel effects.

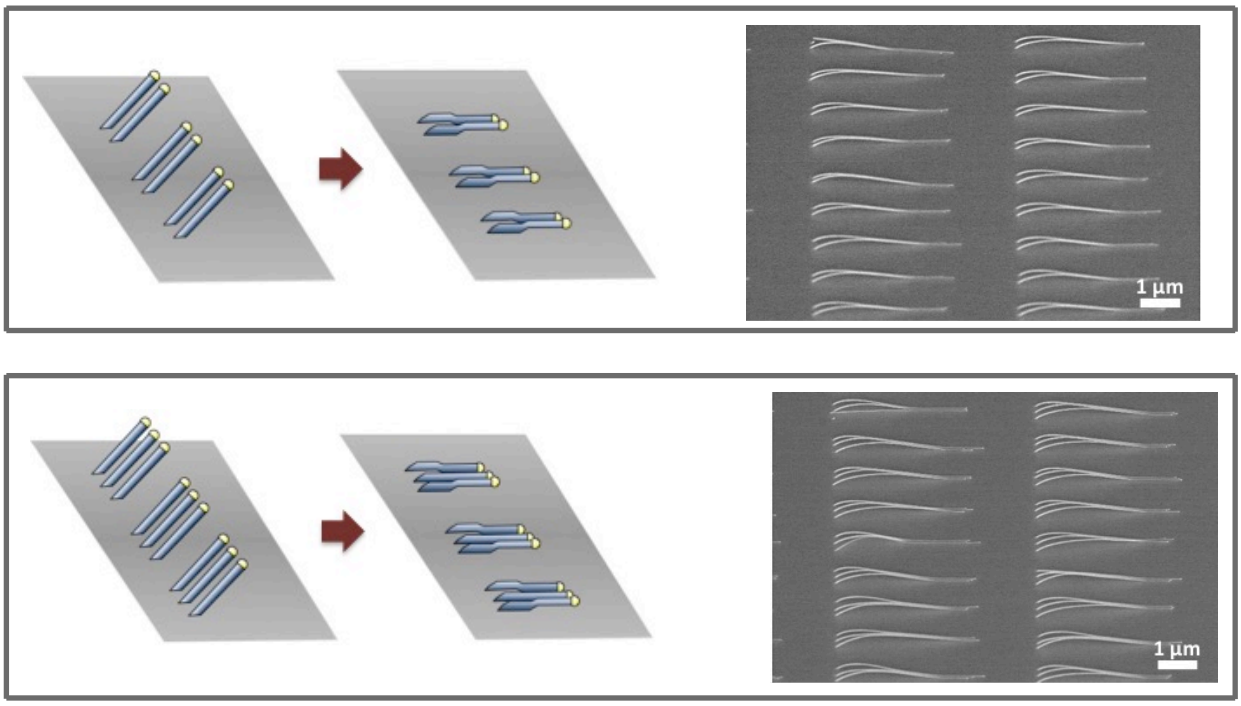

Figure 3.5 Illustration and SEM images of achieving arrays of double/triple nanowires per site using immersion capillary force between the nanowires.

Figure 3.5 shows an illustration and SEM images of achieving arrays of multiple nanowires per site. By utilizing the immersion capillary force between the nanowires double/triple nanowire arrays with yield of over 98% has been achieved. The multiple nanowire arrays have been obtained by varying the pitch between the nanowires. For both the double and triple nanowire arrays, the pitch between the nanowires in each sites were 200 nm whereas the distance between the closest nanowires in neighboring sites were 800 nm for the double nanowire arrays and 500 nm for the triple nanowire arrays. For single nanowire arrays, it was shown that with ~2 µm long nanowires, the yield of alignment is less than 50% when the pitch between the nanowires were

500 nm, but it can be seen that for multiple nanowires, high yield of alignment can be achieved with 500 nm pitch between the neighboring sites. Note that the length of the nanowires used in multiple nanowire arrays are over 3 μm, which implies that when shorter nanowires are used for the alignment, even higher density of nanowire arrays can be obtained.

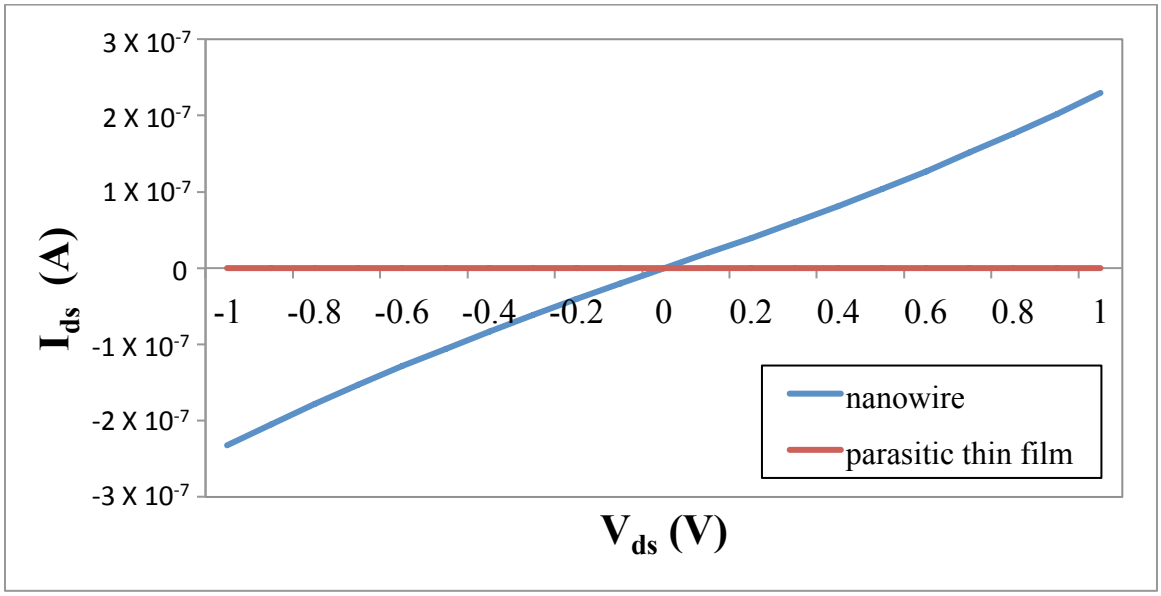

Figure 3.6 Two-terminal measurement of elastocapillary-force aligned nanowire and parasitic film.

Because the nanowires are bent down to the as-grown substrate in elastocapillary-force nanowire alignment, growth of parasitic thin film has to be suppressed while maintaining good growth of the nanowires. Many reports exist on the nanowire device fabrication upon the as-grown substrates. Miao et al. have successfully fabricated high electron mobility transistors using GaAs nanowires grown on GaAs substrate [48]. Parasitic film to nanowire growth ratio was successfully controlled by optimizing temperature and V/III ratio, and the nanowire/film growth rate of over 1000 was reported. Thus, it is possible to grow 2 μm long nanowires while growing parasitic film of only 2 nm thickness. Zhang et al. have grown InAs nanowires on GaAs substrate

with only a few nm parasitic film deposition on the surface [49]. Digital etching was done on the sample to remove the parasitic thin film and MOSFET has been fabricated using the nanowires, proving direct fabrication of the device on an as-grown substrate is possible. To prove the feasibility of direct device fabrication on the elastocapillary-force aligned nanowires, we have grown Si doped GaAs nanowires on semi-insulating GaAs(110) wafers. The diameter of the nanowire was ~70 nm and the length was 5 μm. Two-terminal measurement was done on the nanowires and on the parasitic thin film (Figure 3.6). Although the GaAs nanowire has been successfully doped showing ~0.2 μA current at 1 V bias, the conductance of the parasitic thin film was similar to the semi-insulating substrate showing that there was a negligible amount of parasitic thin film growth during the doped nanowire growth. This proves the feasibility of the elastocapillary nanowire alignment method on the use of direct device fabrication on an as-grown substrate.

CHAPTER 4 – GROWTH OF EPITAXIAL MoS_2 THIN FILMS AND NANOPLATES ON GaN WAFERS

4.1 2-D MoS_2 Growth on GaN Wafers

As mentioned in Chapter 1, without the method to grow single-crystal wafer-scale MoS_2 thin films, mass production of the MoS_2 based devices cannot be realized. To grow single crystal MoS_2 layers, epitaxial growth is needed since it aligns MoS_2 triangles into certain crystallographic orientations. Lattice mismatch is the most important parameter that determines the quality of the epitaxially grown layers, and for the growth of MoS_2, GaN is the best candidate due to the smallest mismatch (<1%) and with hexagonal crystal structure.

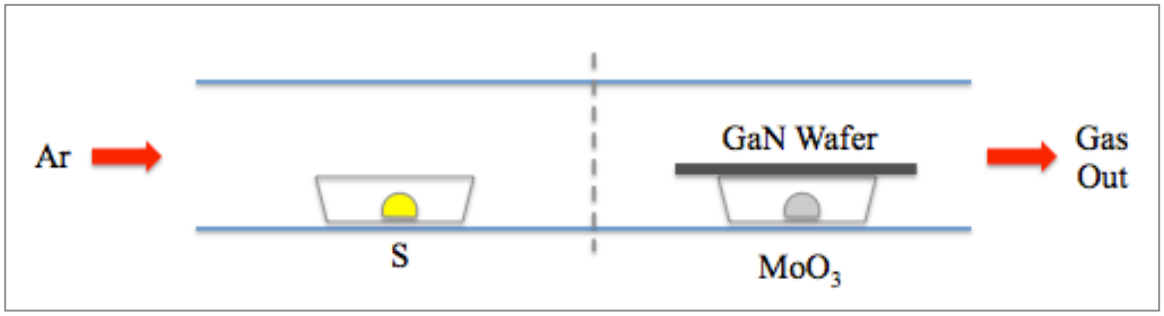

Figure 4.1 Illustration of MoS_2 CVD growth system.

Figure 4.1 shows the CVD growth setup used for the 2-D MoS_2 growth. A two-temperature-zone furnace was used with Ar as a carrier gas. In the upstream, a quartz boat containing sulfur powder was placed and in the downstream, a quart boat containing molybdenum oxide powder was placed. A GaN wafer was placed upside down on top of the quart boat containing MoO_3. Before loading into the growth chamber, the GaN wafer was degreased using Acetone, IPA, and DI water followed by hot plate drying of the PTAS which is used as a catalyst for the growth.

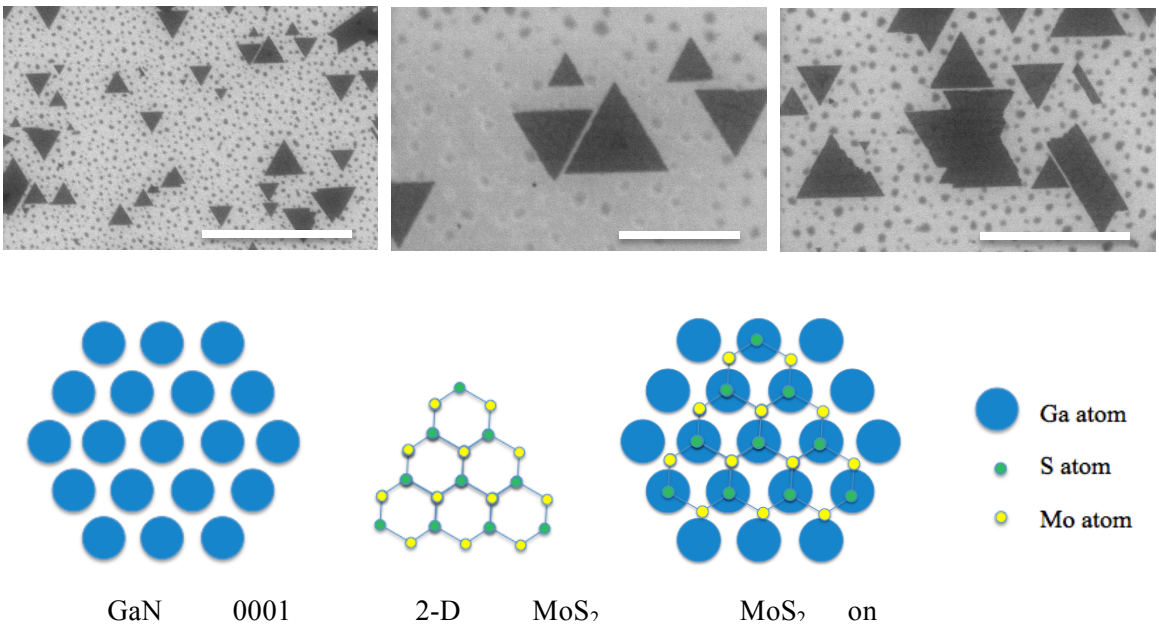

Figure 4.2 (Top) SEM image of the 2-D MoS_2 grown on GaN substrates. The scale bars are (Left) 2 µm, (Center) 500 nm, and (Right) 1 µm. (Bottom) Schematic of the MoS_2 atomic arrangement on the GaN surface.

Figure 4.2 shows SEM images of the MoS_2 triangles grown on GaN substrates. It can be clearly seen that the triangles are aligned in certain directions. Merged triangles can also be seen easily throughout the sample. As mentioned earlier, the mismatch between the MoS_2 and the GaN is very small. MoS_2 has a lattice parameter of 3.16 Å whereas GaN has a lattice parameter of 3.19 Å, which corresponds to ~0.9% lattice mismatch. This allows a good epitaxial growth of the MoS_2 layer on the GaN substrate. Dumcenco et al. have observed similar growth on the sapphire substrate [23], but due to the large lattice mismatch, the alignment ratio of the MoS_2 triangles were significantly lower. Because the MoS_2 triangles grown on GaN substrate show epitaxial behavior with growth in certain crystallographic orientations, the triangles are expected to merge without forming any grain boundaries.

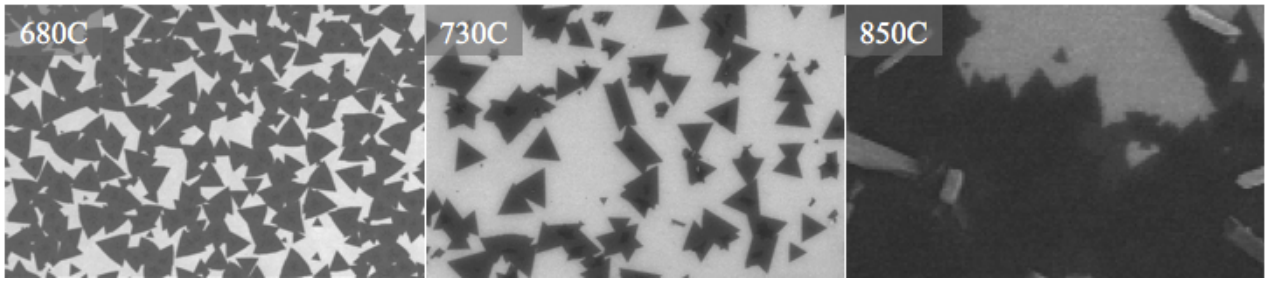

Figure 4.3 SEM images showing the effect of temperature on the MoS_2 growth.

To grow the MoS_2 triangles into a complete film, various growth conditions have been explored. First, temperature dependence of the MoS_2 growth was studied. All of the samples were grown for 5 minutes at the temperature. At 680 ˚C, mostly monolayer MoS_2 grows. As the growth temperature gets higher, it can be seen that more layers grow on top of the initial monolayer MoS_2. In Figure 4.3(center), darker contrast within the MoS_2 triangles show the second layer of MoS_2 being grown on top of the monolayer MoS_2. Thus, it can be seen that the growth at lower temperature is preferable in order to obtain monolayer MoS_2. Note that the alignment of the MoS_2 triangles is not good in Figure 4.3 although the growth condition is the same as in Figure 4.2. It is mainly due to the memory effect which is caused by the material deposition on the quartz camber surface during the prior growths. Thus, the cleanliness of the growth chamber is critical in obtaining a well-aligned epitaxial MoS_2 on the GaN substrates.

With the alignment of MoS_2 on GaN substrates, the next step is to grow a continuous film with uniform thickness in a large scale. Figure 4.4 shows the evolution of MoS_2 growth on the GaN substrate with increased growth time. It can be clearly seen that with more and more growth time, the size of the MoS_2 triangles become larger and become merged to form a continuous layer. Another important parameter of the MoS_2 growth is the density of the PTAS. We have observed that with the higher density of the PTAS, less time is required to form a continuous

film. The density of the PTAS can be controlled either by the amount of PTAS deposited on the substrate or the drying method of the PTAS. Hotplate drying of the PTAS results in relatively higher density of the PTAS leading to higher density of the MoS_2 on the substrate but with less uniformity throughout the substrate. Blow drying of the PTAS using a nitrogen gun results in less dense PTAS but creates uniform PTAS density throughout the substrate.

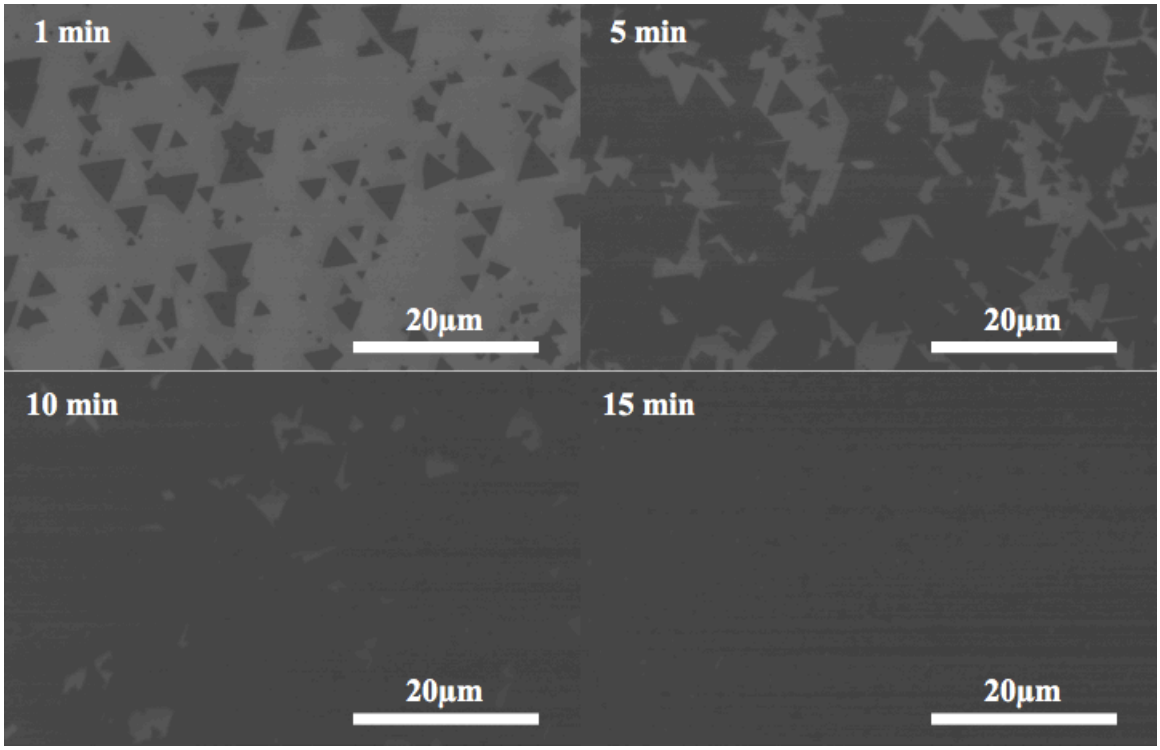

Figure 4.4 SEM images showing time evolution of the MoS_2 growth on a GaN substrate. The growth was done at 680 ˚C with 15 sccm of Ar flow. PTAS was used in all of the samples. With ~15 min growth, MoS_2 grows into a continuous film. Brighter contrast shows GaN substrate whereas darker contrast shows MoS_2 crystals.

To characterize the MoS_2 films grown on GaN substrates, Raman and PL analysis was carried out. As shown in Figure 4.5, two distinct Raman shift peaks can be observed at 383cm^{-1} and 405cm^{-1}, which corresponds to monolayer thickness of MoS_2. A strong PL signal was obtained on the MoS_2 monolayer on the GaN substrate, which is evidence that the MoS_2 is indeed in 2-D shape and not in the bulk form since bulk MoS_2 is known to show a PL signal at a

much lower energy (1.23 eV). Raman and PL mapping of different regions on the substrate would be done in the future to further characterize the uniformity and the quality of the MoS_2 layers grown. Table 4.1 shows growth parameters used for MoS_2 growth.

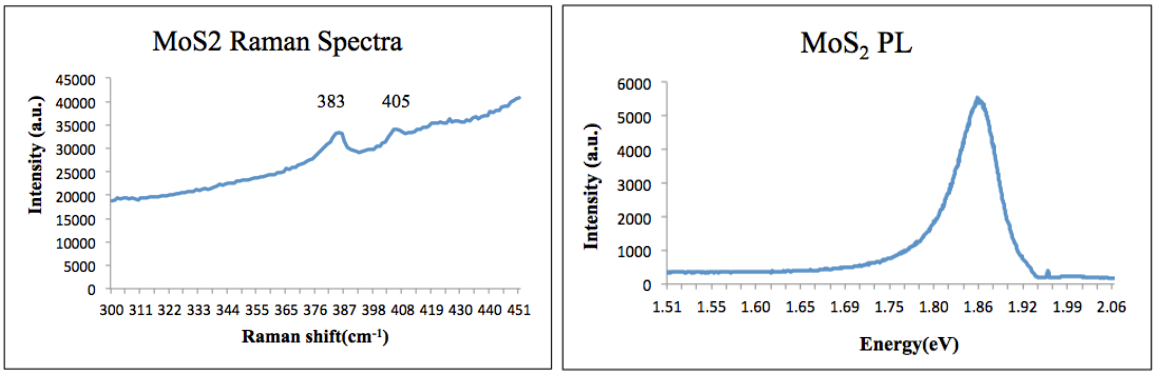

Figure 4.5 (Left) Raman spectra on the MoS_2 film grown on GaN substrate. (Right) Photoluminescence spectra of the MoS_2 film grown on GaN substrate.

Table 4.1 MoS_2 growth parameters and observed morphology.

Temperature (°C)	Growth Time (min)	PTAS	Ar Flow (sccm)	Substrate	MoS_2 Morphology
680	1	O	15	GaN	monolayer triangle low density
680	5	O	15	GaN	monolayer triangle high density
680	10	O	15	GaN	monolayer near continuous film
680	15	O	15	GaN	monolayer continuous film
730	5	O	15	GaN	multilayer triangle low density
800	1	O	15	GaN	multilayer continuous film
800	10	X	15	GaN	Multilayer continuous film
730	10	X	15	GaN	monolayer/bilayer continuous film
730	15	O	15	SiO_2	circular shape, nearly monolayer not epitaxial
730	15	O	400	SiO_2	multilayer continuous film not epitaxial

4.2 Nanoplate Growth on GaN Wafers

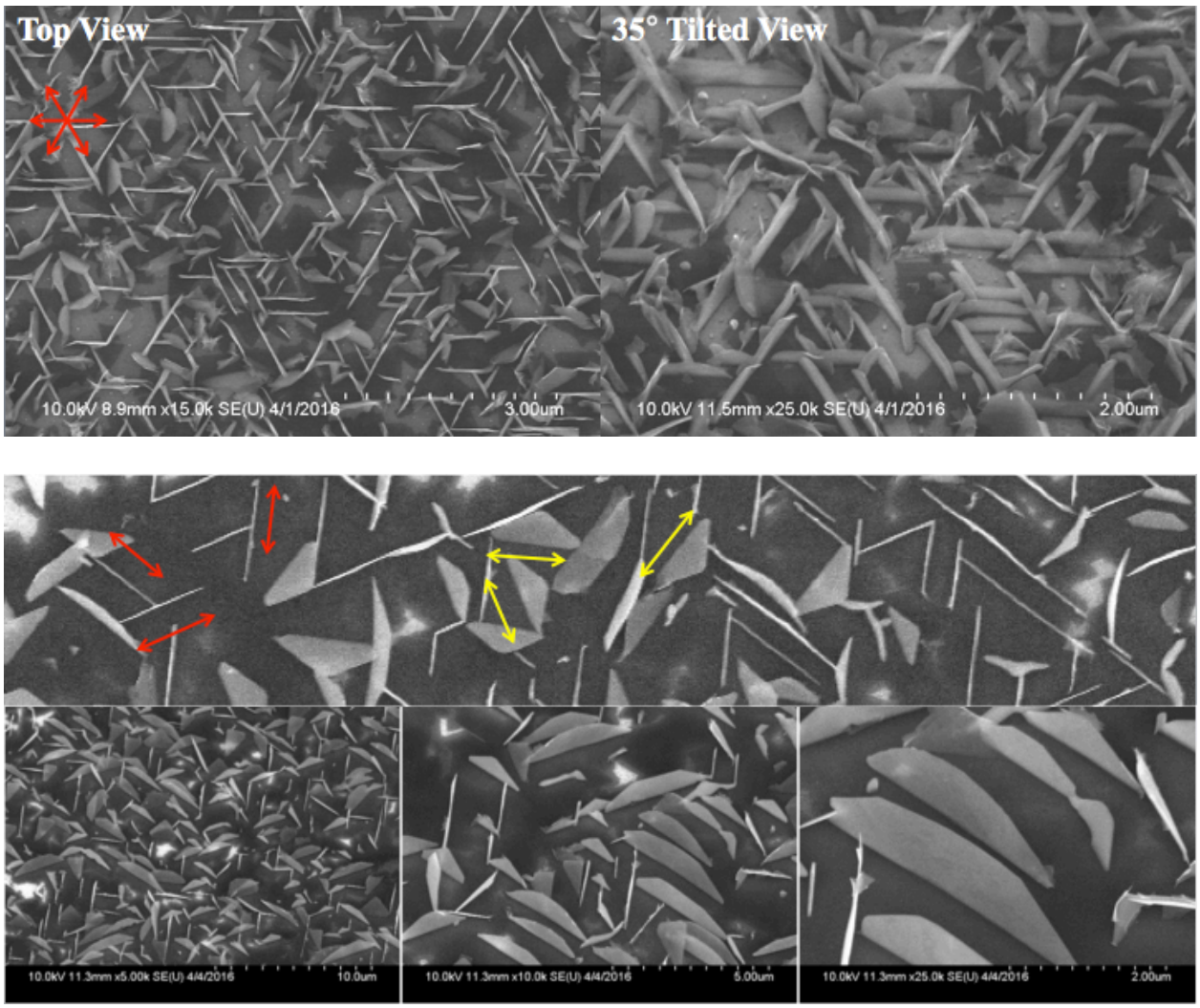

Figure 4.6 (Top) Nanoplates grown at 800 ˚C for 15 minutes. Red arrows indicate the orientation of the nanoplates. (Bottom) Nanoplates grown at 730 ˚C for 30 minutes. Two types of nanoplates can be seen. Vertical nanoplate alignment orientation is indicated by red arrows and tilted nanoplate alignment orientation is indicated by yellow arrows.

We now explore the MoS_2 structure change beyond the complete film formation. Figure 4.6 shows an SEM image of a sample grown at 800 ˚C for 15 minutes and a sample grown at 730 ˚C for 30 minutes. Unique MoS_2 nanoplates can be observed everywhere on the growth substrate. At 800 ˚C, it can be seen that most of the MoS_2 nanoplates are grown vertically (Figure 4.6 top). The base of the nanoplates is aligned along six equivalent <1 1 -2 0> orientations on the

hexagonal (0001) surface. On the other hand, at 730 ˚C, two types of distinctive nanoplates can be seen (Figure 4.6 bottom). One type of nanoplates are grown vertically with the base of the nanoplate aligned in <1 1 -2 0> orientations whereas the other type of nanoplates are tilted relative to the substrate and are aligned in <1 0 -1 0> directions. The thickness of the thinnest nanoplates were beneath the measurable point under SEM which is ~ 5 nm. The shape of the nanoplates was also different between different types. Nanoplates aligned in <1 1 -2 0> were trapezoidal whereas the nanoplates aligned in <1 0 -1 0> were pentagon shaped. The different shapes are due to the energetics of the facets in different crystallographic planes. From the contrast between the MoS_2 films beneath the nanoplates and the exposed GaN substrate, it can be seen that the nanoplates are grown on multi-layer MoS_2 films. Figure 4.7 shows nanoplates with longer growth time. It can be seen that the nanonoplates have become thicker but not any taller or longer. For 5 minute growth, the nanoplate thickness was below 5 nm whereas for 10 minute growth, the nanoplate thickness was measured to be ~ 20 nm. HAADF/STEM EDX was carried out for composition analysis. Because the EDX peak of Mo and S overlap, the composition of the nanoplates is hard to be determined. It is certain that the nanoplate contains Mo atoms, but S may or may not be in the nanoplates. We believe that the nanoplate is either MoS_2 or MoO_3 since no other atoms exist in the growth chamber. Optical and electrical characterization will be done in the future to analyze the composition of the nanoplates. Table 4.2 shows growth parameters used for nanoplates and observed morphology.

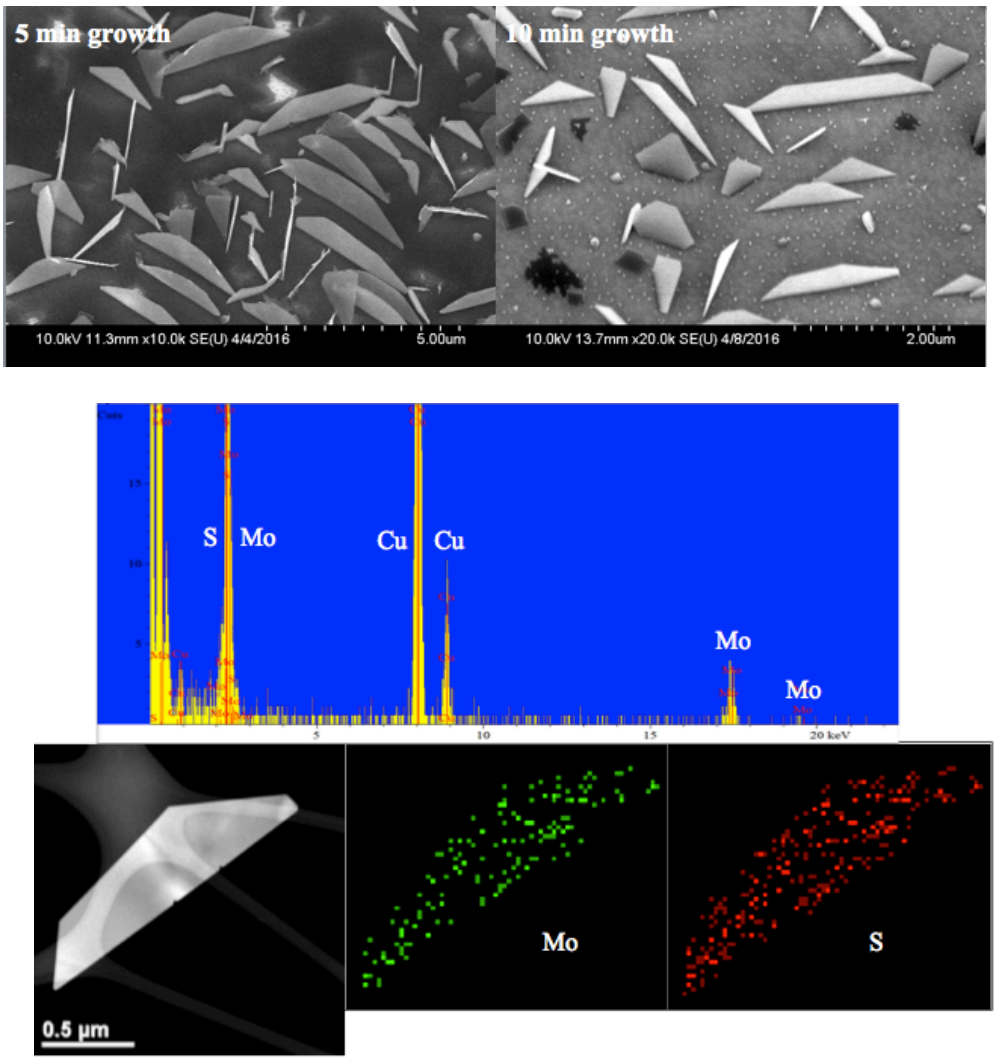

Figure 4.7 (Top) Comparison of nanoplates with different growth time. (Bottom) HAADF/STEM image and EDX of the nanoplate.

Table 4.2 Nanoplate growth parameters and observed morphology.

Temperature (°C)	Growth Time (min)	PTAS	Ar Flow (sccm)	Substrate	MoS_2 Morphology
730	30	O	15	GaN	multilayer continuous film thin nanoplates
800	15	O	15	GaN	multilayer continuous film thick nanoplates
850	5	O	15	GaN	multilayer continuous film thick nanoplates

4.3 MoS_2-GaN Diode

To date, no report exists on the fabrication of an electrical device with MoS_2 grown on GaN. To characterize the property of the MoS_2 grown on GaN substrates, we have fabricated a MoS_2-GaN pn diode. Because the conduction band minimum of MoS_2 lies low relative to the vacuum, n-type doping is expected to be observed in native MoS_2 [50]. Thus, to form a pn junction, we have grown continuous film of MoS_2 on a p-type GaN substrate. Although some reports show that the MoS_2 growth on p-type GaN results in degradation of the MoS_2 crystal quality [24], we observe similar MoS_2 morphology as on n-type GaN.

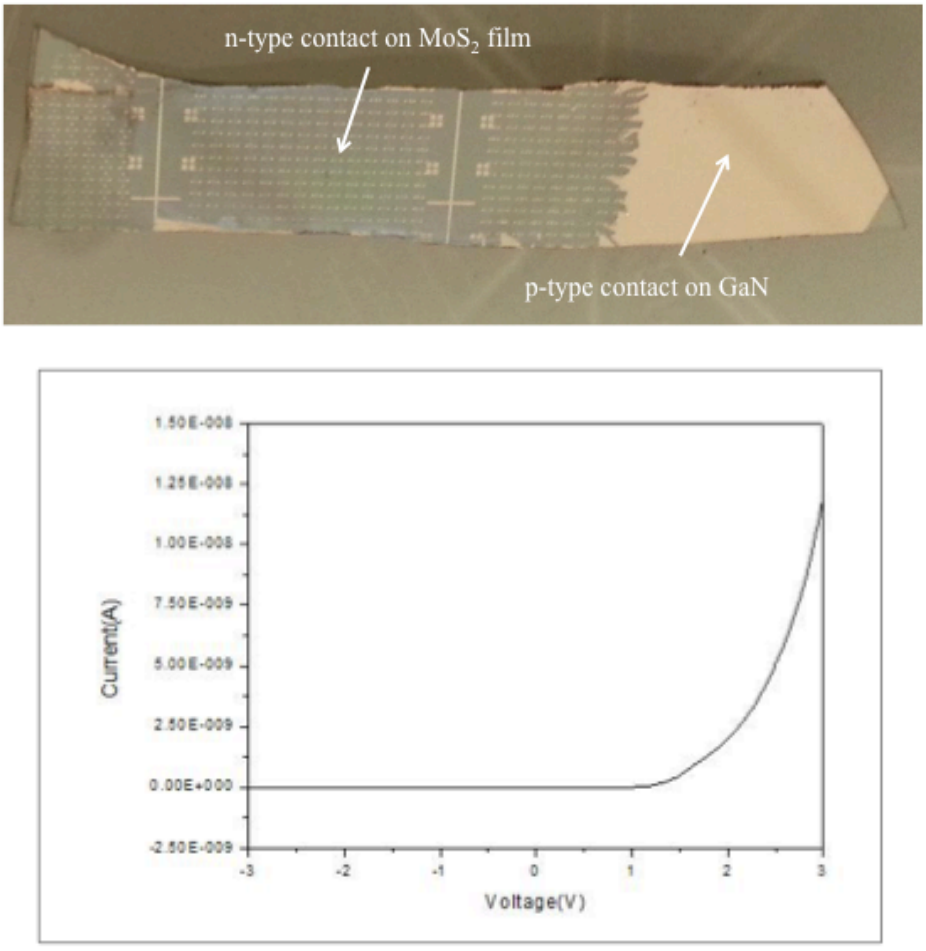

Figure 4.8 Photograph of an n-MoS_2/p-GaN diode and a plot showing current-voltage characteristics of the diode.

For the growth of MoS_2 for the n-MoS_2/p-GaN diode, CVD growth was done at 730 ˚C for 10 minutes. A continuous layer of mono/bilayer film was grown under the condition. The size of the continuous film was ~1 cm X 0.5 cm. Optical lithography was done on the sample to make metal contact on the MoS_2 and the p-GaN substrate. For the contact metal, 10 nm/100 nm/10 nm thickness of Ni/Au/Ni was deposited using an ebeam evaporator.

As shown in Figure 4.8, clear diode behavior can be observed, which proves that the MoS_2 grown on GaN is indeed n-type. The turn-on-voltage of the diode matches the bandgap of the few-layer-MoS_2 in the literatures. The calculated ideality factor is ~6 which is probably due to the distance between the contacts (>1 cm). Although a report exists on the fabrication of a MoS_2/GaN diode [51], the diode was fabricated by transferring MoS_2 onto GaN substrate. Our diode differs in the aspect that the device was fabricated directly on the as-grown substrate, and thus we expect the quality of the interface between the MoS_2 and the GaN to be much better.

CHAPTER 5 – FUTURE WORKS

5.1 Arrays of III-V Nanowires on Silicon

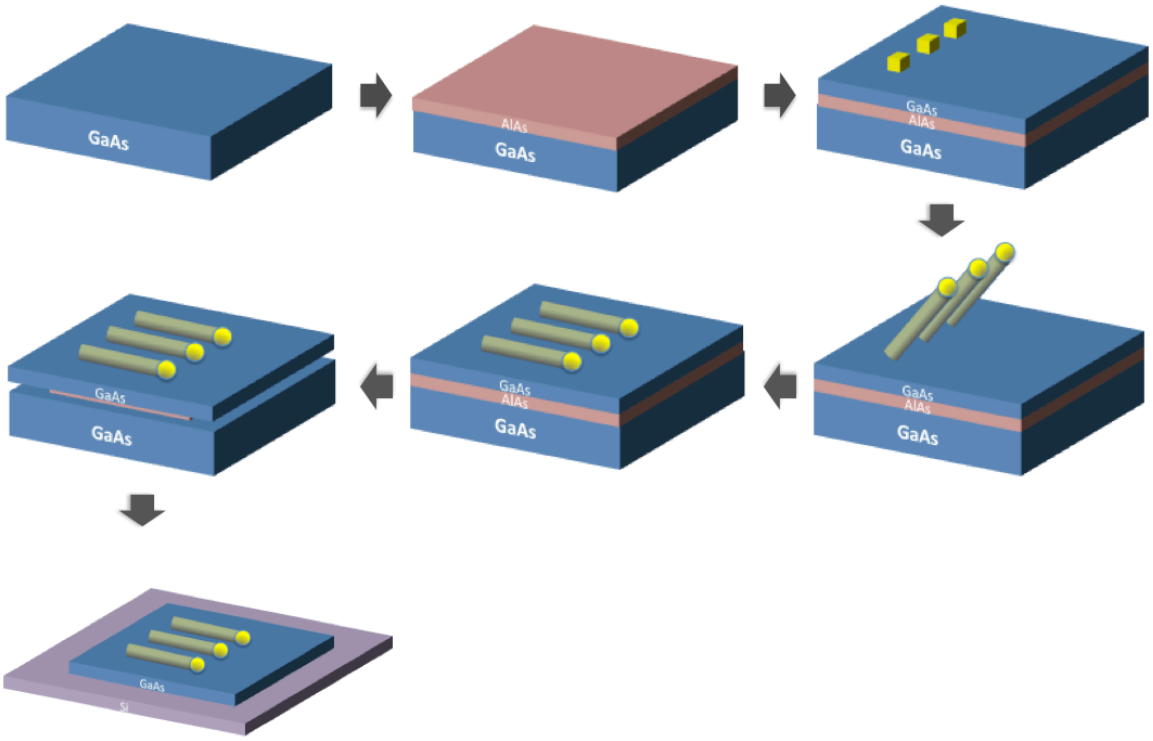

Figure 5.1 Process of transferring arrays of III-V nanowires onto silicon.

In order for industries to adopt III-V nanowire array transistors, it is preferable to transfer the III-V nanowires onto silicon since the industry is more familiar with silicon technology. Also, it is much more efficient in terms of cost to transfer the III-V nanowires onto silicon rather than using the III-V wafer itself for the fabrication of transistors.

Figure 5.1 shows the III-V nanowire transfer process onto silicon. Because aluminum has a similar lattice parameter to gallium (<1% difference), AlAs or AlGaAs sacrificial layers can be grown onto GaAs substrates followed by thin undoped GaAs film growth. Au catalysts can be patterned onto the GaAs layer by lithography which will be used to grow nanowires in the

MOCVD reactor. As grown nanowires can be aligned into planar fashion using the elastocapillary-force alignment. Then, the sacrificial AlAs/AlGaAs layer will be etched to separate the topmost GaAs layer from the GaAs substrate. The separated GaAs layer with nanowires can then be transferred onto silicon by methods such as microcontact printing. The transferred nanowires can be fabricated into a desired device structure.

5.2 Achieving an Array of Multiple Types of Nanowires

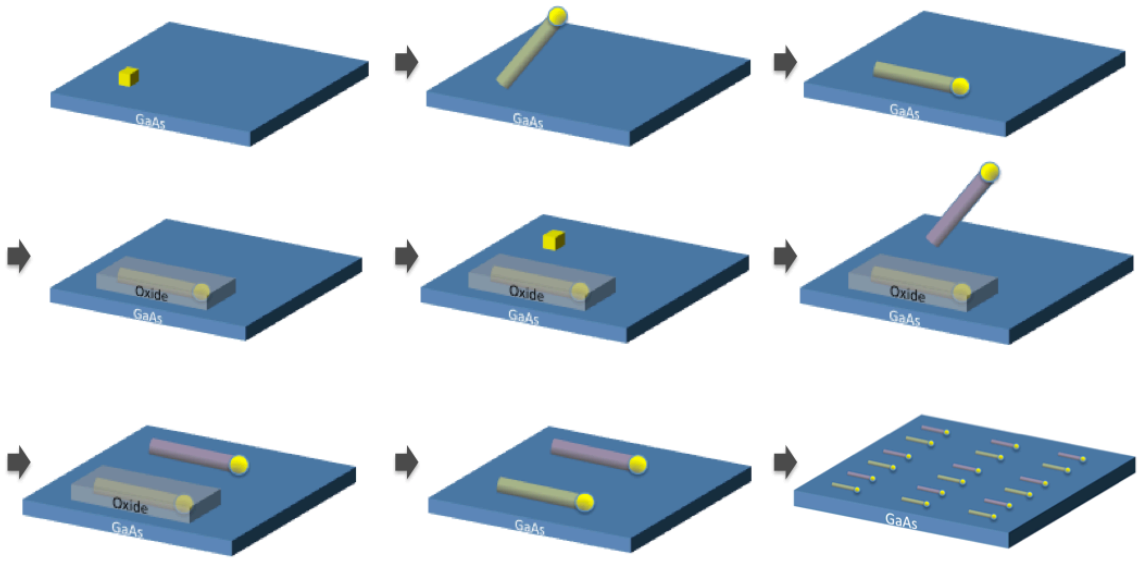

Figure 5.2 Process of achieving an array of multiple types of nanowires.

For some applications, more than one type of nanowires will be needed on a single wafer. For example, it would be preferable to have an array of InAs and GaSb nanowires on a same substrate for CMOS applications since InAs has a high electron mobility whereas GaSb has a high hole mobility. Figure 5.2 shows an illustration of aligning multiple types of nanowires on the same substrate. After the alignment of one type of nanowires, the nanowires can be covered with a protection layer such as oxides. Oxide layers prevent the axial growth of other materials at

the residual catalyst as well as protecting the nanowire surface from deposition or desorption of materials. After the oxide deposition over the first set of nanowires, a second set of gold catalysts can be patterned and other types of nanowires can be grown out of the catalysts. The second set of nanowires can be laid down onto the substrate to form arrays as well using the same approach as the first nanowires. The oxides then can be removed to form an array consisting of two different type of nanowires. As long as the parasitic thin film growth can be suppressed, more than two types of nanowires can be formed into arrays by repeating the previous steps.

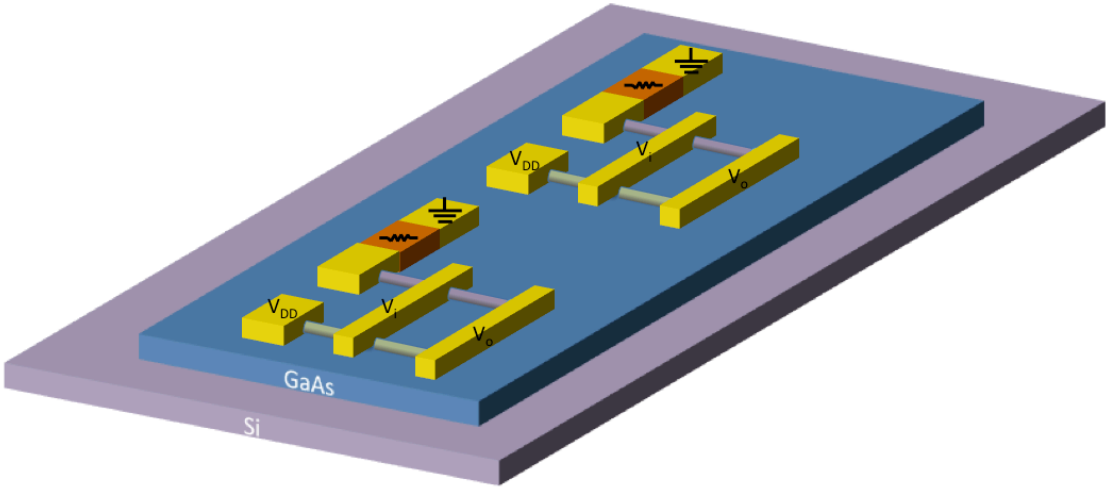

Figure 5.3 Illustration of wafer-scale logic circuits fabricated from aligned III-V nanowires and transferred onto silicon.

The ultimate goal of nanowire alignment research is to fabricate wafer-scale transistor chips comprised of nanowire channels. Figure 5.3 shows wafer-scale logic circuits fabricated by aligned nanowires transferred onto silicon substrate. By combining the nanowire aligning approaches in the previous sections and transferring it onto a foreign substrate, wafer-scale logic

circuits that are comprised of III-V nanowires can be fabricated on any substrates. Also, by transferring the nanowires onto flexible substrates, flexible devices can be made.

5.3 Wafer-Scale Single-Crystal Growth of MoS_2

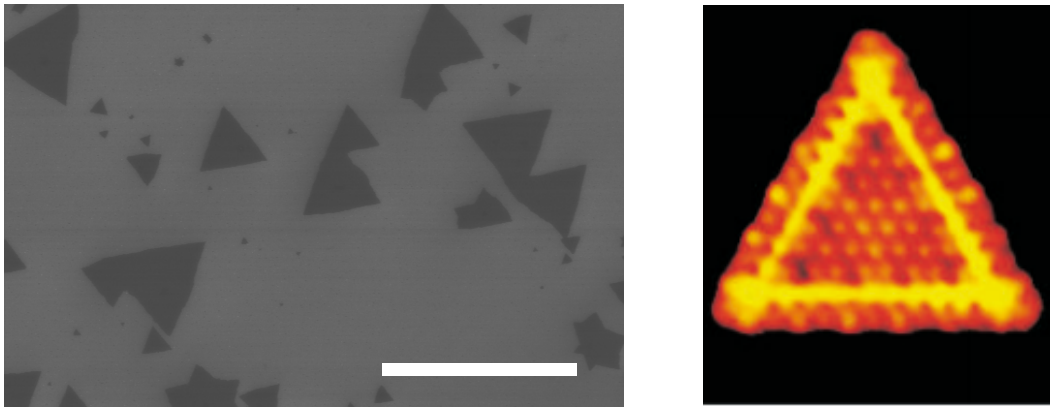

Figure 5.4 (Left) SEM image of merged MoS_2 triangles grown on a GaN substrate. Scale bar is 10 μm. (Right) STM image of a MoS_2 triangle. Adapted by permission from Macmillan Publishers Ltd: *Nature Nanotechnology*, Reference [52], copyright (2007).

In Chapter 4, we have shown the epitaxial growth of the aligned MoS_2 triangles on the GaN substrates and their evolution into a continuous film. In order for the MoS_2 based devices to be mass produced, it is critical to achieve uniformity throughout the entire film without having any grain boundaries. Although we have shown aligned MoS_2 triangles on GaN substrates, the yield of the aligned triangles was less than 95%. The non-aligned triangles would cause grain boundaries when merged into a continuous film. We observed that the yield of the alignment is dependent on the temperature, surface state of the GaN substrate, and the density of the PTAS. Thus, it is important to control these parameters to increase the MoS_2 alignment yield. Also, since the second layer of the MoS_2 starts to grow once the triangles merge into a continuous film, it is critical to control the density of the PTAS or find a condition for monolayer MoS_2 growth without using PTAS.

Although, we assume that if the aligned MoS_2 triangles merge into a film no grain boundaries would exist, no one has actually characterized the interface between the merged triangles. Figure 5.4 shows a SEM image of merged MoS_2 triangles grown on GaN substrate. STM analysis on the interface between triangles would give clear evidence on whether there would be a grain boundary at the merged interface. Moreover a STM analysis on the continuous MoS_2 film would demonstrate whether a single-crystal MoS_2 film is grown or not.

For growing uniform continuous monolayer MoS_2 film, optimization of the growth temperature and time is needed. Also, it is preferable to find a growth condition that does not require PTAS since it is hard to have a uniformly dispersed PTAS on wafers which would then lead to non-uniform growth on the substrate. Thus, along with the optimization of MoS_2 triangle alignment conditions, uniform monolayer MoS_2 growth condition optimization will be varied in the future.

5.4 Nanoplate Characterization

The nanoplates grown on GaN substrates have not been fully analyzed. As mentioned in Chapter 4, since EDX peaks of Mo and S atoms overlap, other characterization tools are needed in order to clarify its composition.

If the nanoplates are MoO3, they can be used as cathodes in battery applications. Also, if the nanoplates are MoS_2, the crystallographic orientation will be different from 2-D planar (0 0 0 1) films, and the optical and electrical properties would be completely different. Figure 5.5 shows a HRTEM image of a vertical nanoplate with trapezoidal shapes. Atomic planes can be clearly seen which implies that the MoS_2 nanoplates are indeed single crystalline. The atomic plane distance in Figure 5.5 (right) is measured to be 0.16 nm which implies that if the nanoplate is

indeed MoS_2, the planes in the TEM image are (1 0 -1 0) planes, and unlike in 2-D MoS_2 films which has alternating layers of Mo atoms and S atoms, the nanoplates would contain both the Mo and S on the same atomic plane.

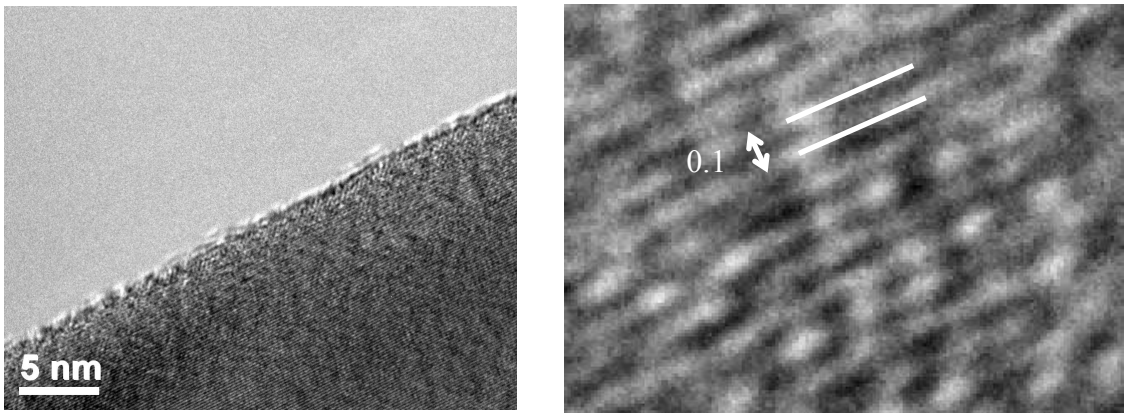

Figure 5.5 HRTEM image of a nanoplate.

For the future study, complete TEM characterization will be done on the nanoplates to identify the crystallographic orientation. PL and Raman will be done on the transferred MoS_2 nanoplates to characterize the optical property. Devices such as MOSFETs will also be made to measure the electrical properties of the nanoplates.

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